

# ASUS CONFIDENTIAL

MODEL NAME : *Elsa*

PCB NO : ???

ASUS P/N : ???

## Lanai UMA Schematics Document

uFCPGA Mobile Merom  
Intel Crestline-GM + ICH8M

2007-03-19

REV :1.2(DELL: X02)

MB PCB

Part Number	Description
DAB00004H0L	PCB 00B LA-3071P REV0 M/B

*BOM NO. ???*

*PCB P/N: ???*

PROJECT:

REVISION

1.2

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DESCRIPTION:

*Cover Page*

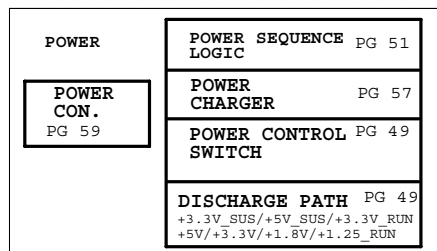
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RELEASE DATE :

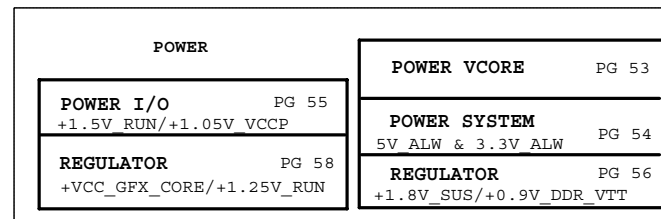
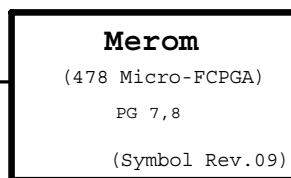
DESIGN ENGINEER :

# LANAI: UMA

**CLOCK**  
CK410M+LP  
PG 21

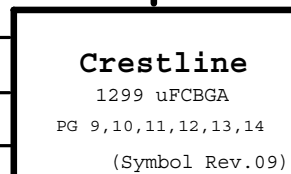


**SDP**  
PG 52



**Panel Connector**  
PG 28

LVDS

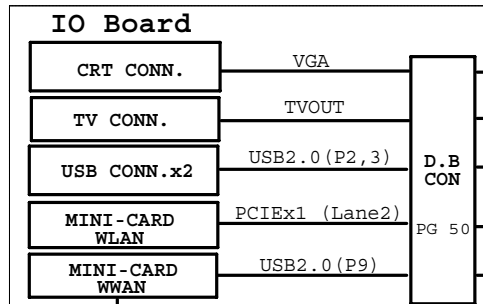


533/667 MHZ DDR II

**DDR2-SODIMM1**  
PG 19

533/667 MHZ DDR II

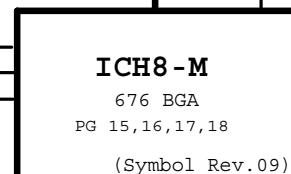
**DDR2-SODIMM2**  
PG 19



DMI INTERFACE

USB2.0 (P0,P1)

**USB CONN.**  
PG 39  
**USB Board**



PCIE (Lane6)

PCI

PCIE (Lane4)

USB2.0 (P6)

USB2.0 (P7)

**CARD READER**  
1394/R5C833  
PG 32,33,34

**BCM5906KMLG**  
QFN-68 PG 47

IHDA

USB2.0 (P5)

**CAMERA**  
PG 28

SATA

**SATA-HDD**  
PG 31

IDE

**CD-ROM**  
PG 31

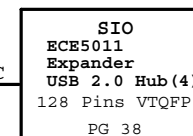
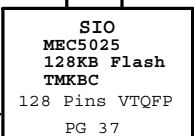
**EXPRESS-CARD**  
R5538  
PG 35

**RJ45/Magnetic**  
PG 48

**Bluetooth**  
PG 41

SPI

LPC



BC

**CIR**  
PG 41

**FLASH**  
PG 40

**Touchpad CON.**  
PG 41

**FAN & THERMAL**  
EMC4001  
PG 43

**USER INTERFACE**  
PG 42

**SNIFFER**  
PG 42

**CAPBTN CON.**  
PG 40

**AUDIO/AMP**  
PG 44,45,46

**MDC**  
PG 36

**S/PDIF TO TV CONN.**  
PG 30

**DIGITAL MIC.**  
PG 28

**Speaker CON**  
PG 46

**WtoB CON**  
PG 46

**Audio Jacks \*3**  
**JACK Board**

**RJ11**

**RJ11 Board**

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DESCRIPTION:  
**BLOCK DIAGRAM**

SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER :

A	B	C	D	E
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11

### Footprint Definition

Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

### Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

### PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

### PCI Express TABLE

Lane 1	WWAN / Mini Card
Lane 2	WLAN / Mini Card
Lane 3	
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5906KMLG

### USB TABLE

ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	User2 (Single port , in USB BD)
ICH8-2 (EHCI#1)	User3 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User4 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	
ICH8-5 (EHCI#1)	Camera
ICH8-6 (EHCI#2)	ExpressCard
ICH8-7 (EHCI#2)	BT Module
ICH8-8 (EHCI#2)	
ICH8-9 (EHCI#2)	WWAN / Mini Card

Note : No USB for WLAN

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DESCRIPTION:

Bus Connection

SCHEMATIC FILE NAME :

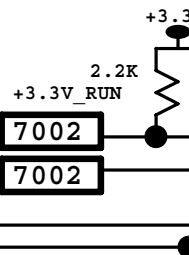
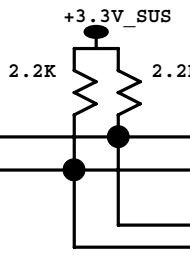
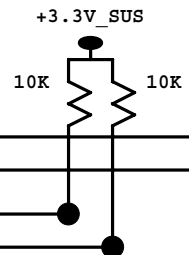
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DESIGN ENGINEER :

RELEASE DATE :

ICH8-M

AJ26 ICH\_SMBCLK  
AD19 ICH\_SMBDATA  
AC17 AMT\_SMBCLK  
AE19 AMT\_SMBDAT



MEM\_SCLK 197  
MEM\_SDATA 195  
MEM\_SCLK 197  
MEM\_SDATA 195

DIMM 0  
DIMM 1

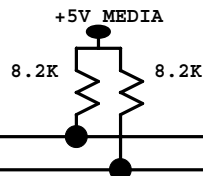
I/O Board

Express Card

WWAN

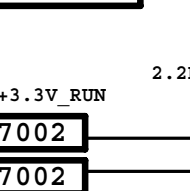
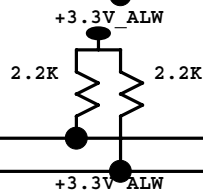
WLAN

6 DOCK\_SMBCLK  
5 DOCK\_SMBDAT



CAPBTN Board

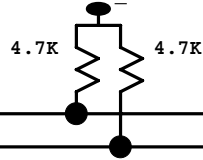
13 CKG\_SMBCLK  
12 CKG\_SMBDAT



CLK\_SCLK 16  
CLK\_SDATA 17

CLK GEN.

100 THRM\_SMBCLK  
99 THRM\_SMBDAT

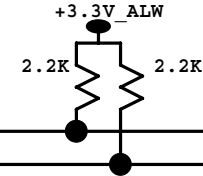


+3.3V\_ALW

12  
11

ECE4001

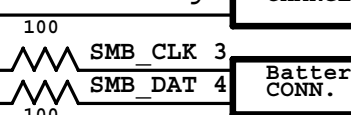
112 PBAT\_SMBCLK  
111 PBAT\_SMBDAT



+3.3V\_ALW

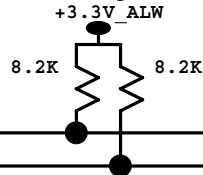
10  
9

CHARGER



Battery  
CONN.

8 LCD\_SMBCLK  
7 LCD\_SMBDAT

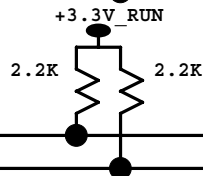


+3.3V\_ALW

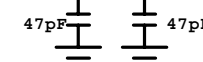
34  
35

LVDS  
Connector

LCD\_DDCCLK  
LCD\_DDCDAT



+3.3V\_RUN



43  
44

VGA

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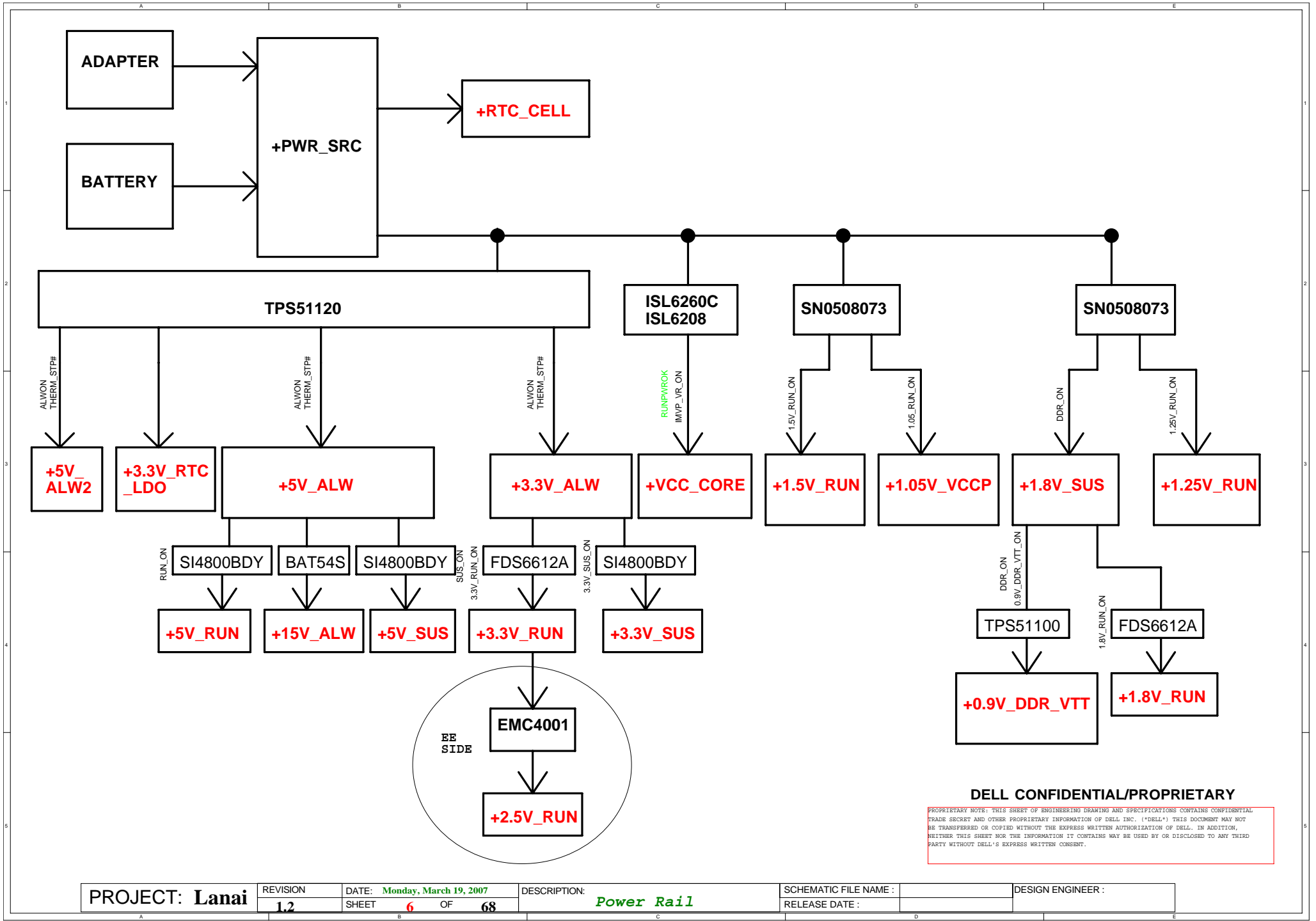
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DESCRIPTION:  
SMBUS BLOCK

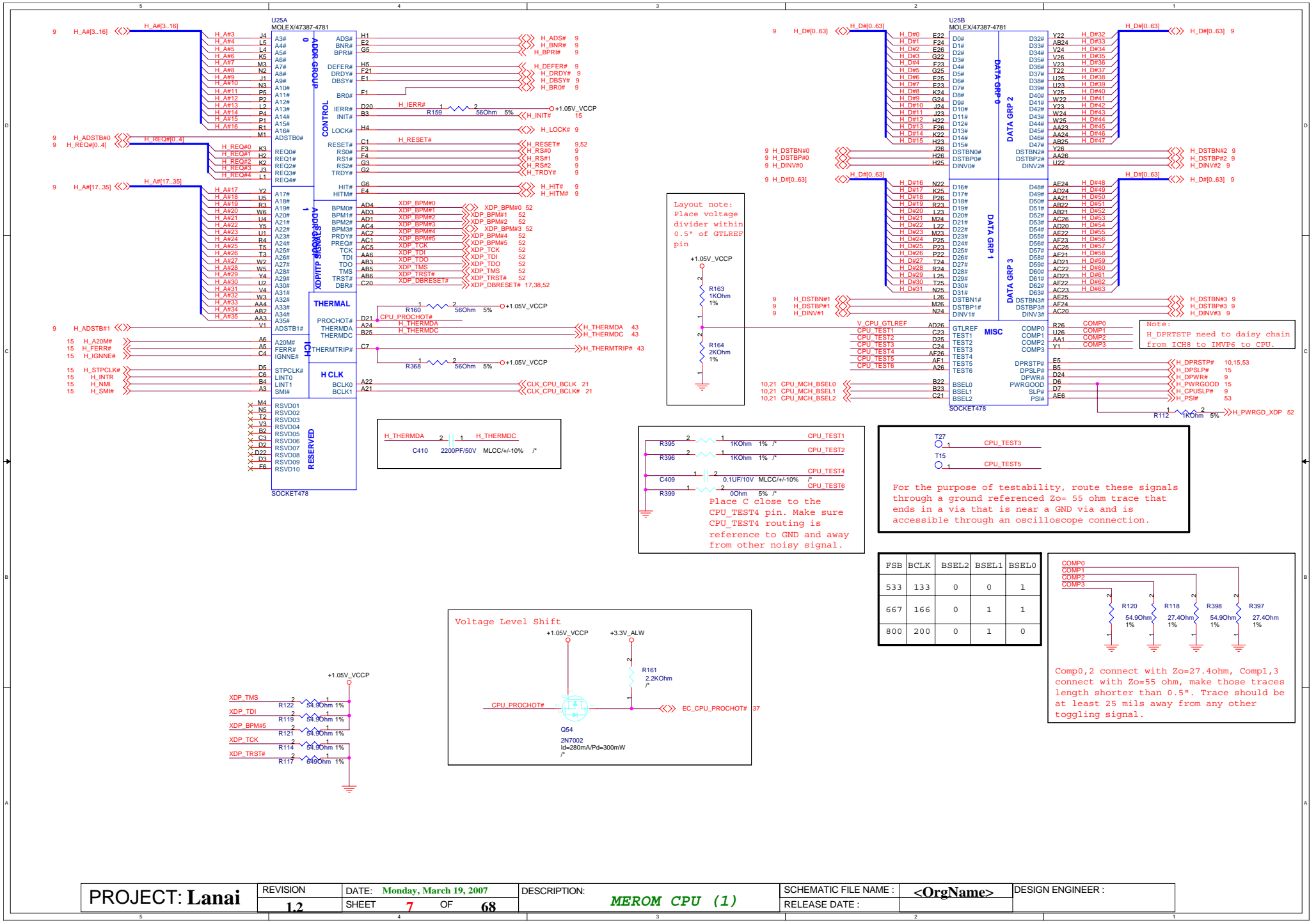
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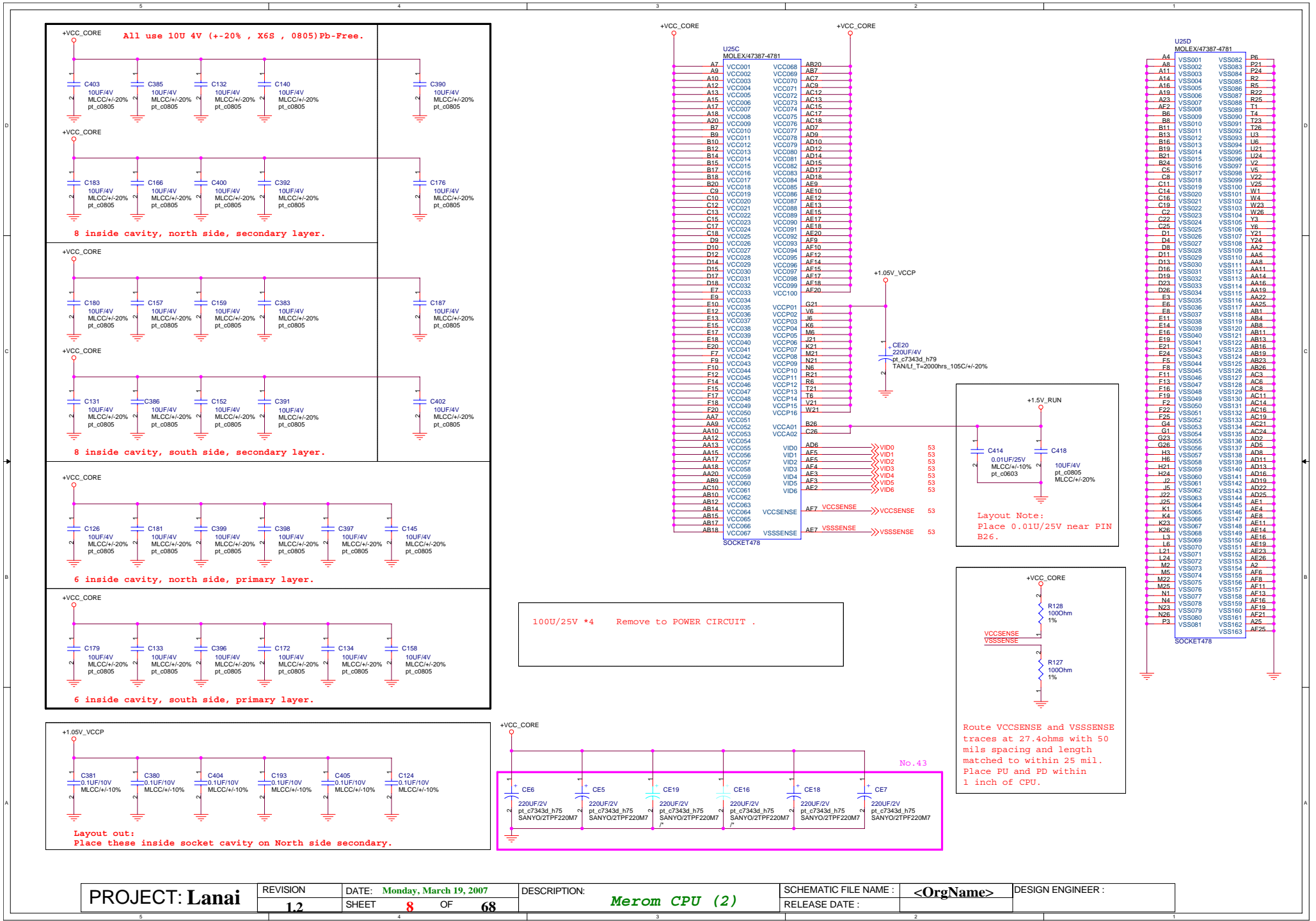
DESIGN ENGINEER :



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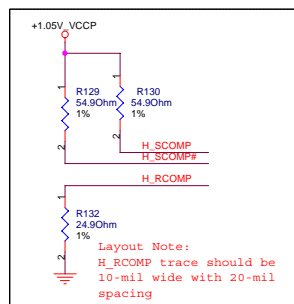
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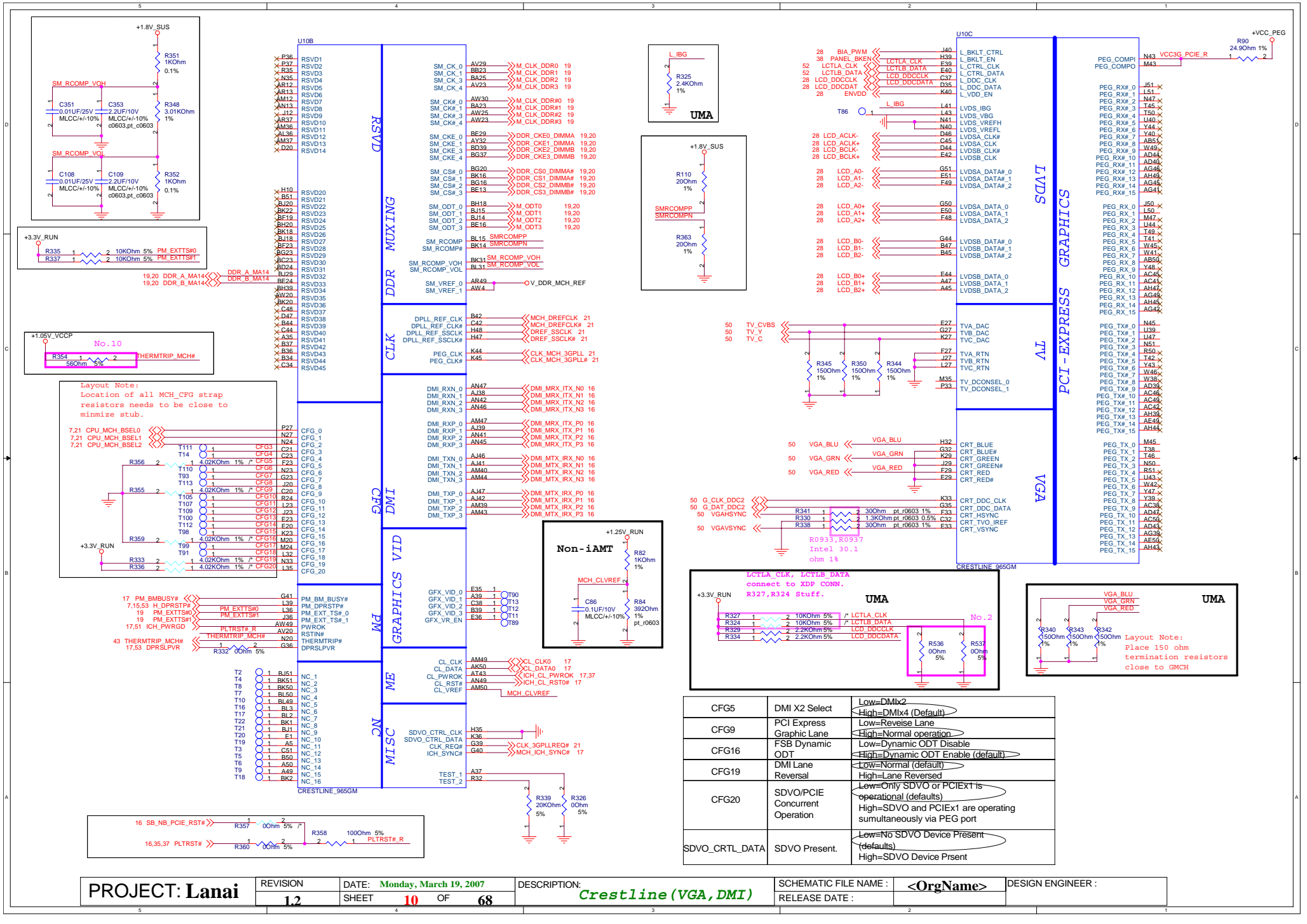
DESCRIPTION: Merom CPU (2)

SCHEMATIC FILE NAME: <OrgName>  
RELEASE DATE:

DESIGN ENGINEER:







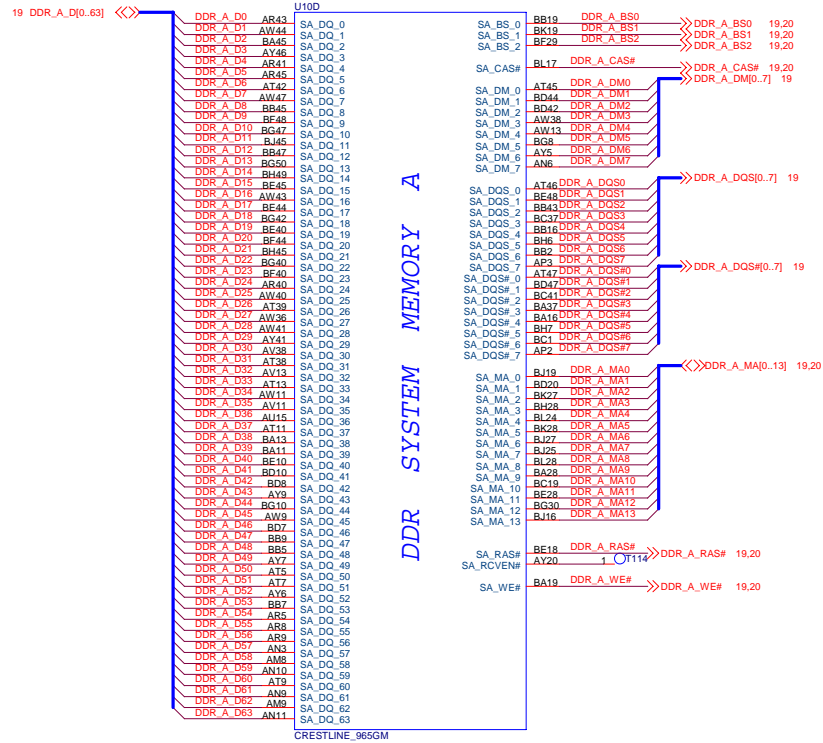
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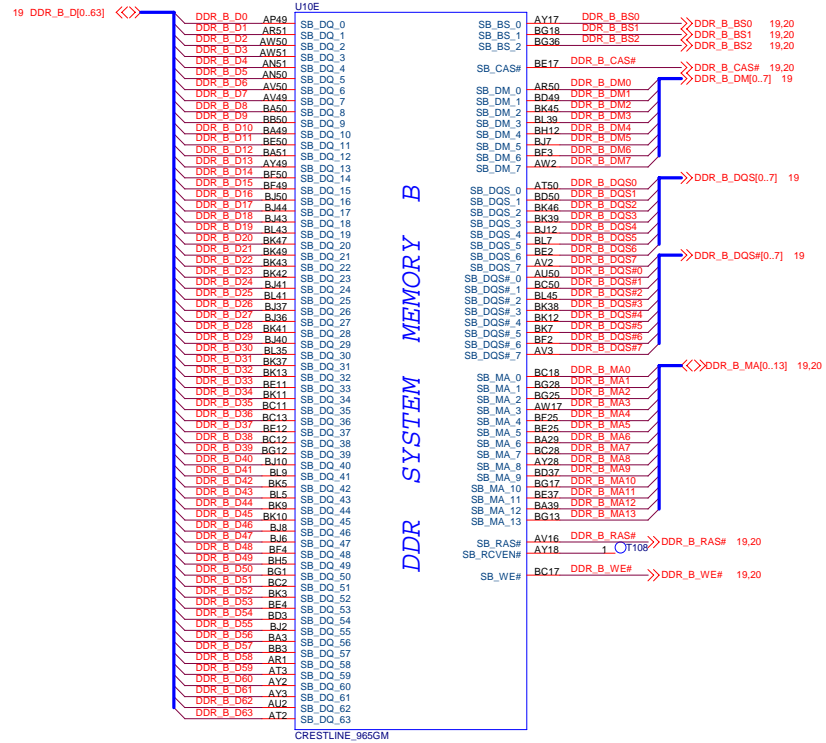
DATE: Monday, March 19, 2007  
DESCRIPTION: Crestline (VGA, DMI)

SCHEMATIC FILE NAME: <OrgName>  
RELEASE DATE: DESIGN ENGINEER:

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIe Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (defaults) High=SDVO Device Present



DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

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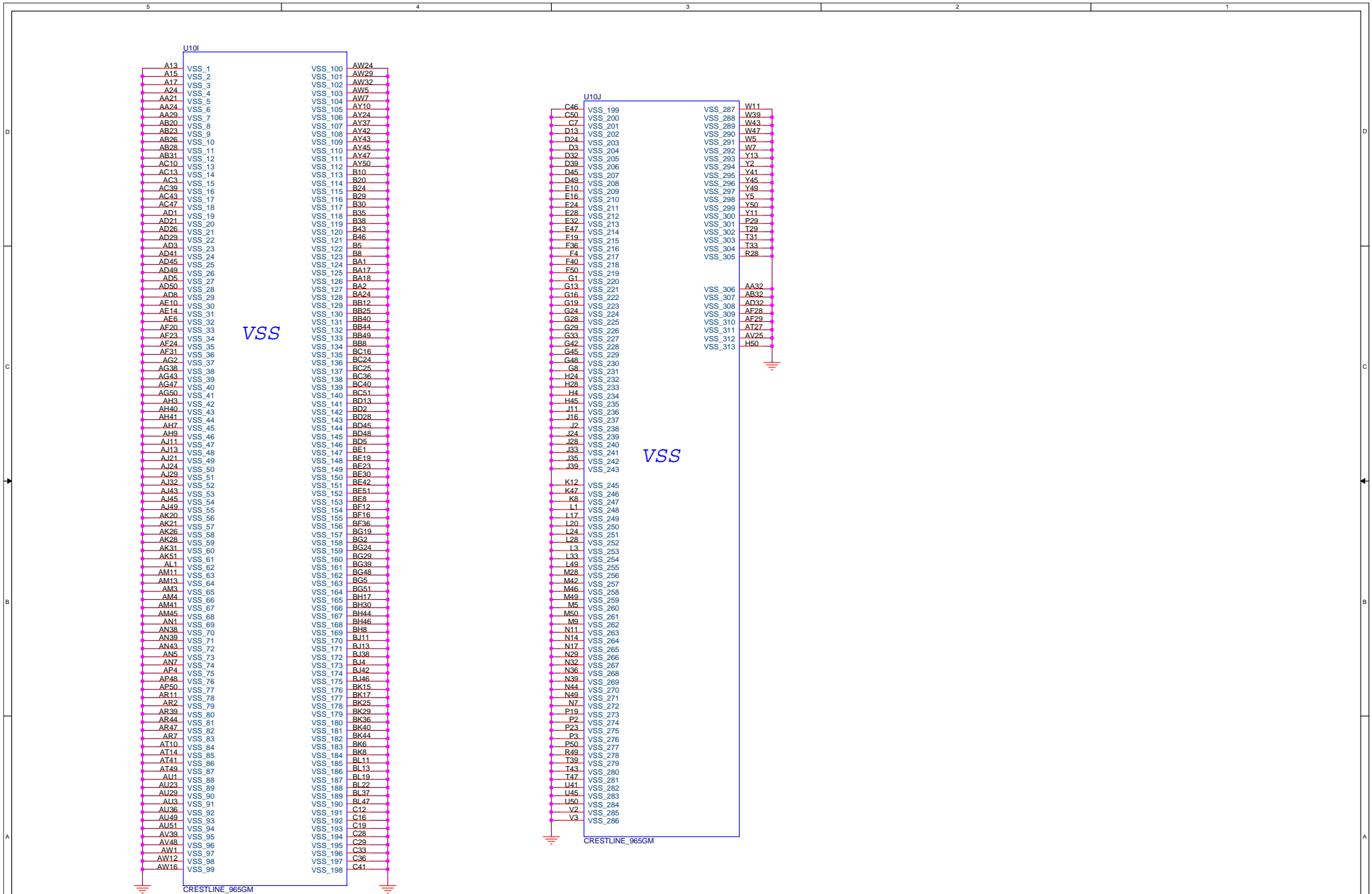
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Crestline (DDR2)

SCHEMATIC FILE NAME : <OrgName>  
RELEASE DATE :

DESIGN ENGINEER :

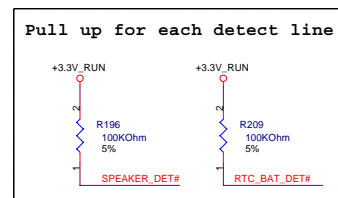
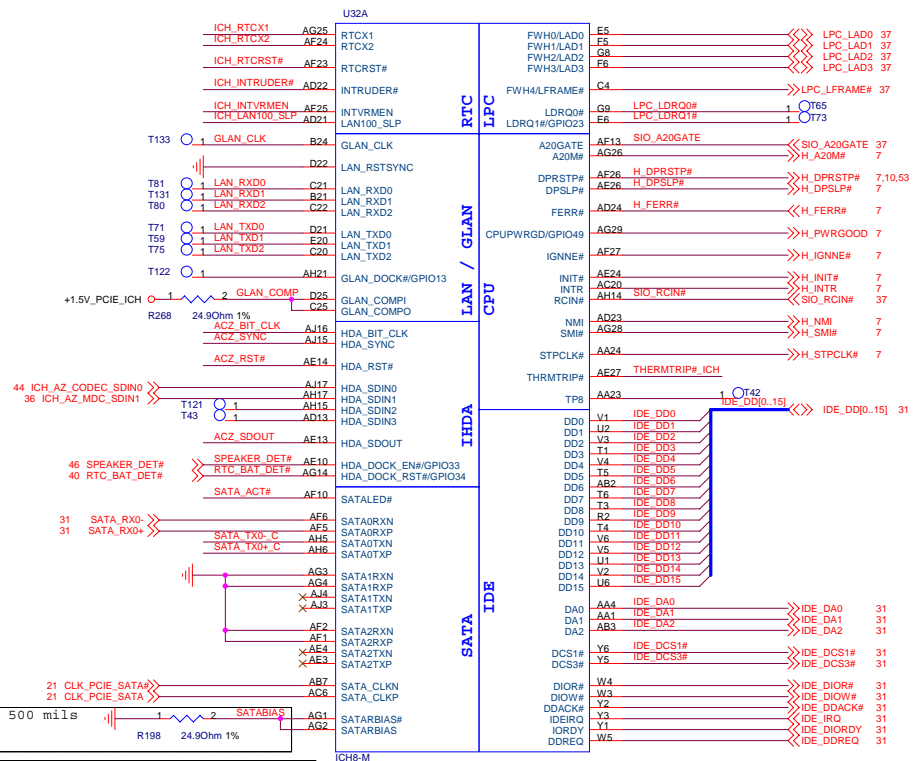
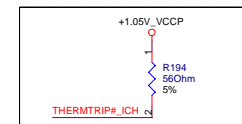
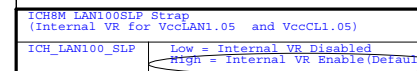
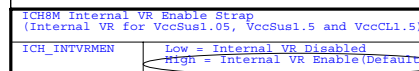
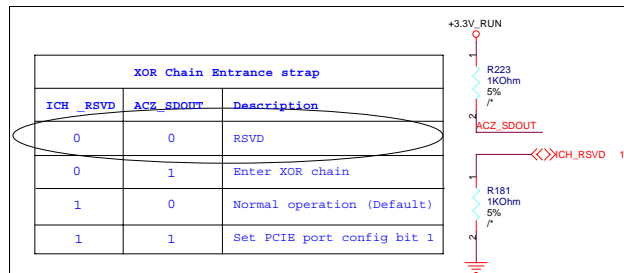
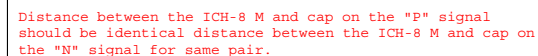
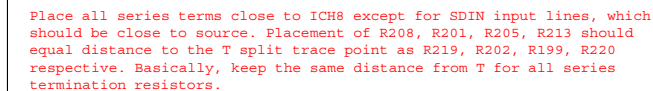
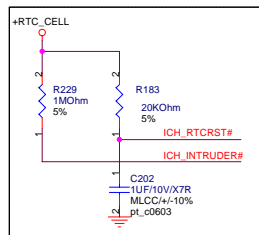
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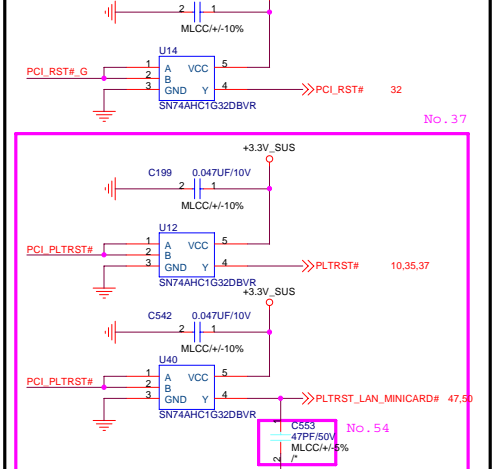
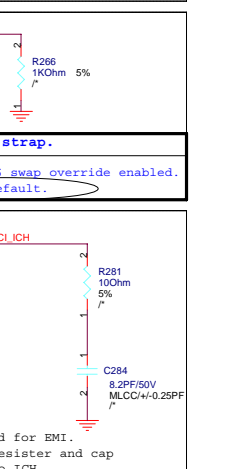
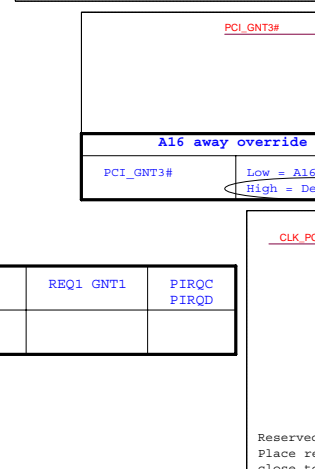
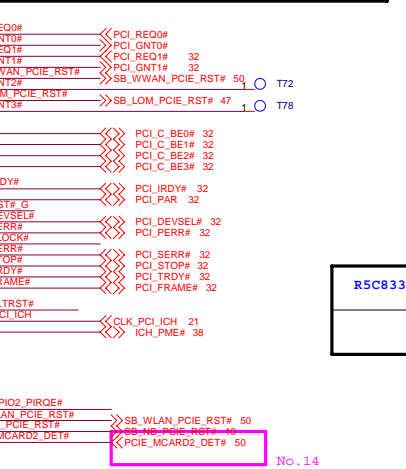
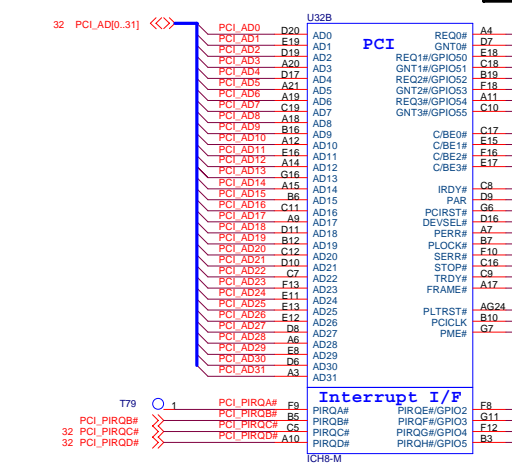
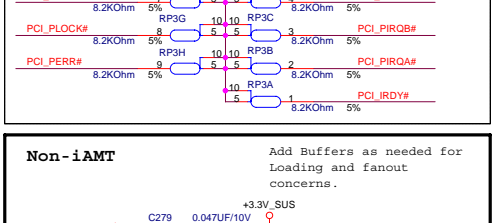
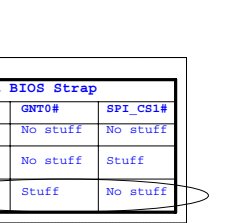
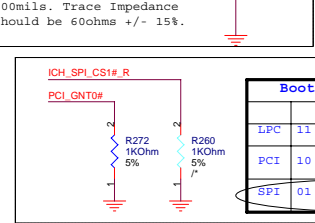
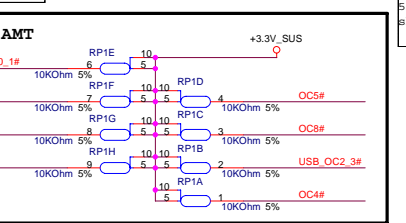
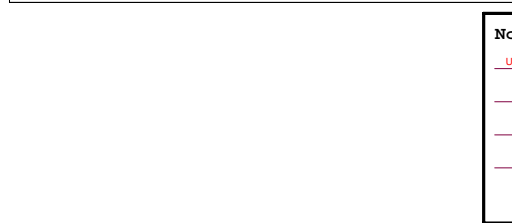
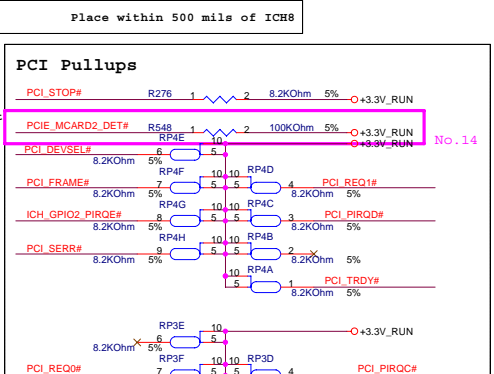
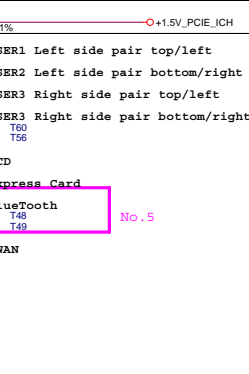
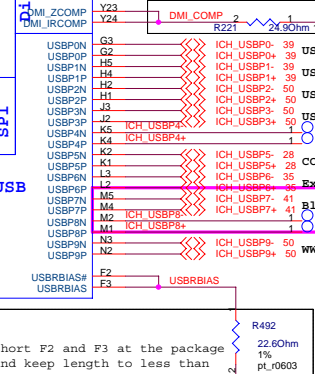
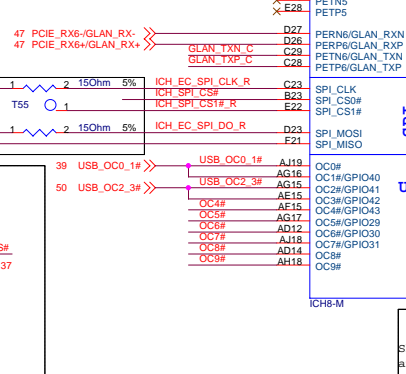
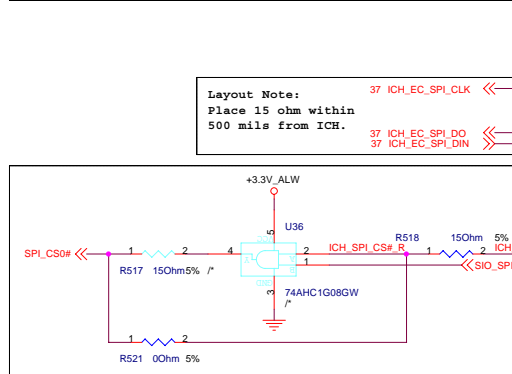
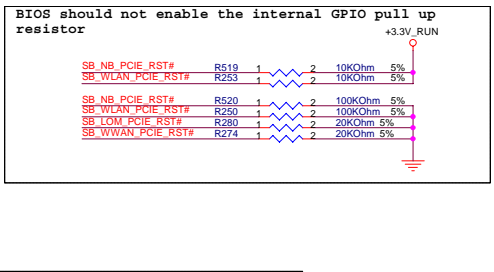
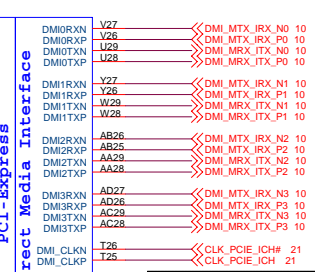
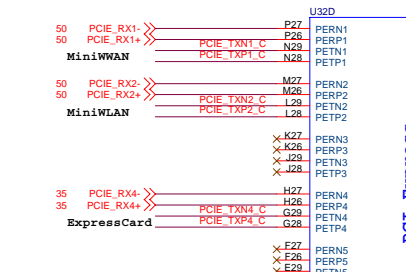
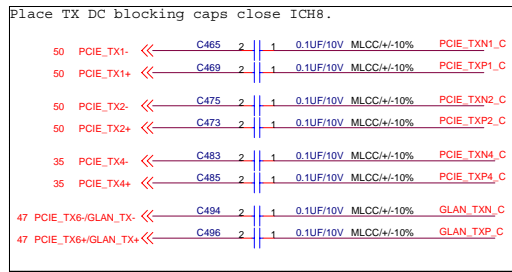




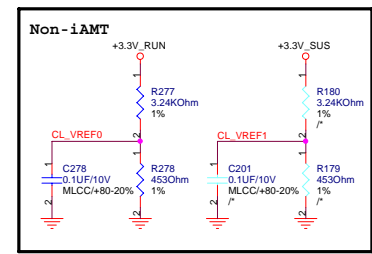
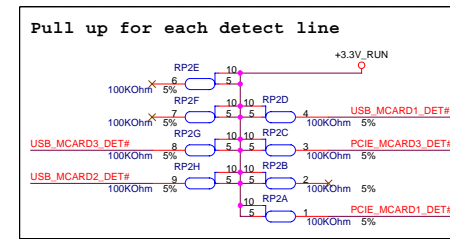
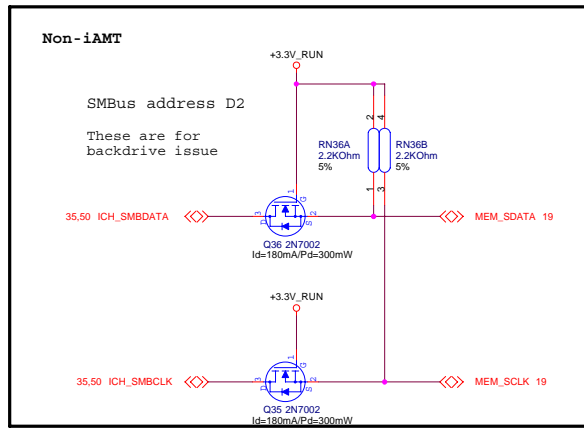
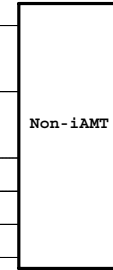
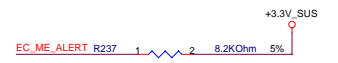
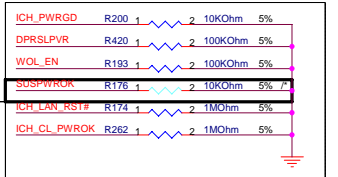
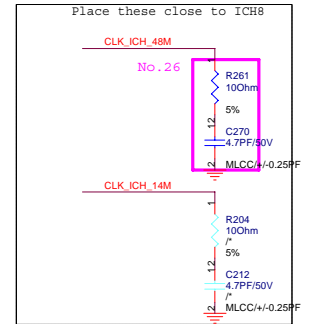
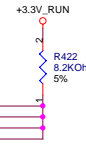
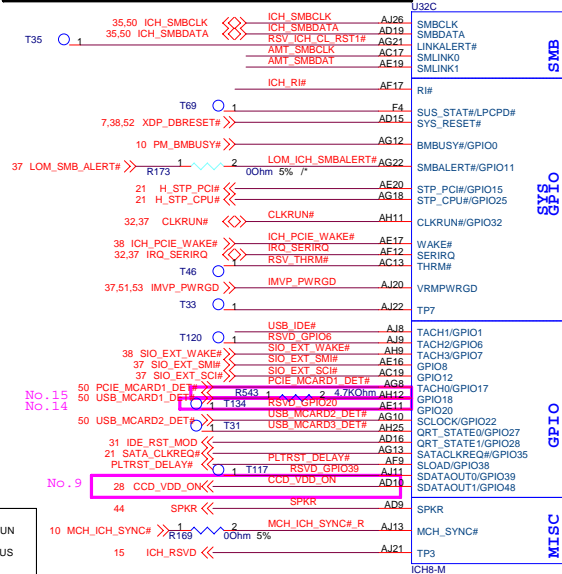
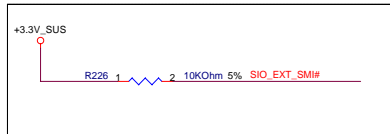
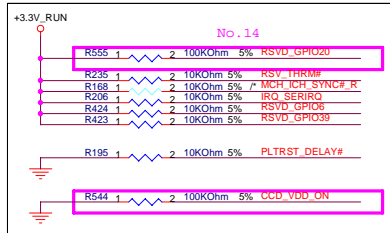
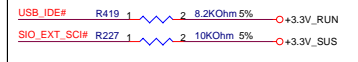
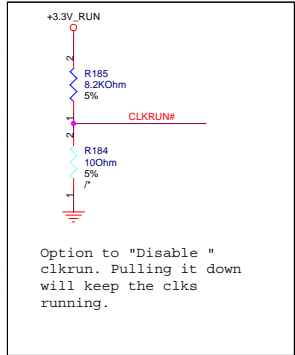
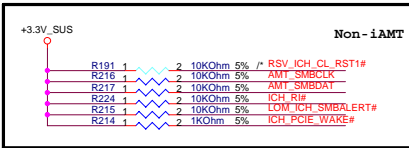
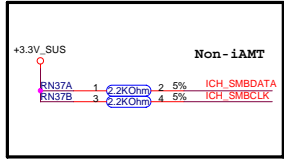
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
	1.2	SHEET 14 OF 68	Crestline (VSS)		







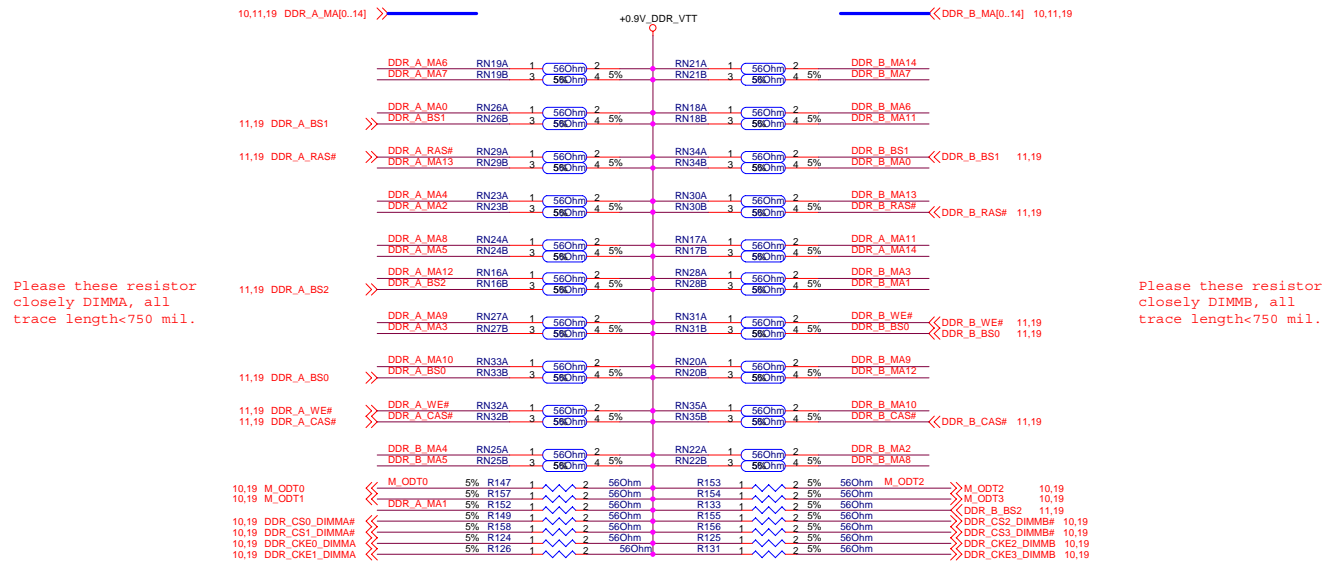
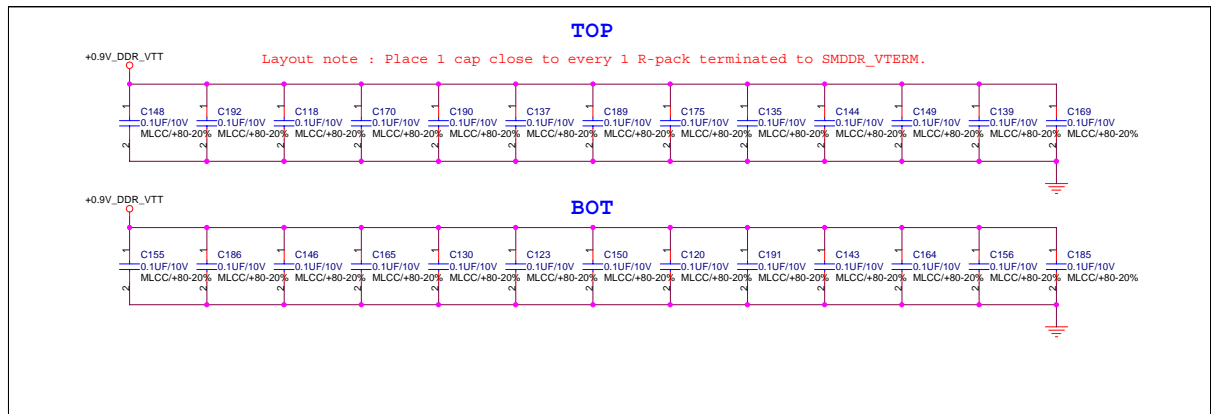




PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME:	<OrgName>	DESIGN ENGINEER:
	1.2	SHEET 17 OF 68	ICH8: SMB/PWR/CLK/GPIO	RELEASE DATE:		







PROJECT: Lanai

REVISION  
1.2

DATE: Monday, March 19, 2007  
SHEET 20 OF 68

DESCRIPTION: DDR2 SO-DIMM (1)

SCHEMATIC FILE NAME: <OrgName>  
RELEASE DATE:

DESIGN ENGINEER:





5					4					3					2					1				
D																								
C																								
B																								
A																								
PROJECT: Lanai					REVISION		DATE: Monday, March 19, 2007		DESCRIPTION:					SCHEMATIC FILE NAME :		<OrgName>		DESIGN ENGINEER :						
					1.2		SHEET 23 OF 68							RELEASE DATE :										
5					4					3					2					1				

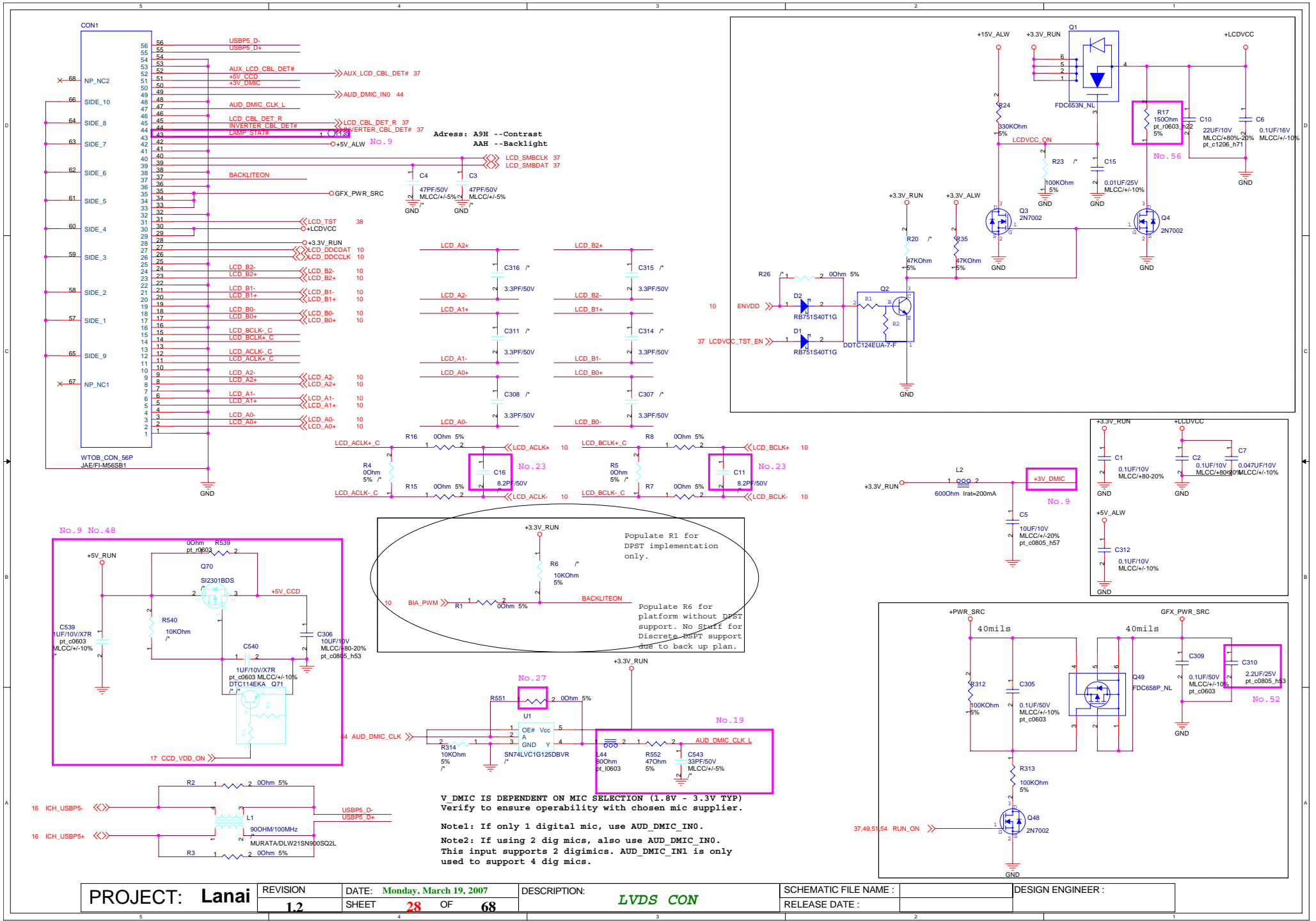
PROJECT: <b>Lanai</b>	REVISION	DATE: <b>Monday, March 19, 2007</b>	DESCRIPTION:	SCHEMATIC FILE NAME :	<b>&lt;OrgName&gt;</b>	DESIGN ENGINEER :
	<b>1.2</b>	SHEET <b>24</b> OF <b>68</b>		RELEASE DATE :		

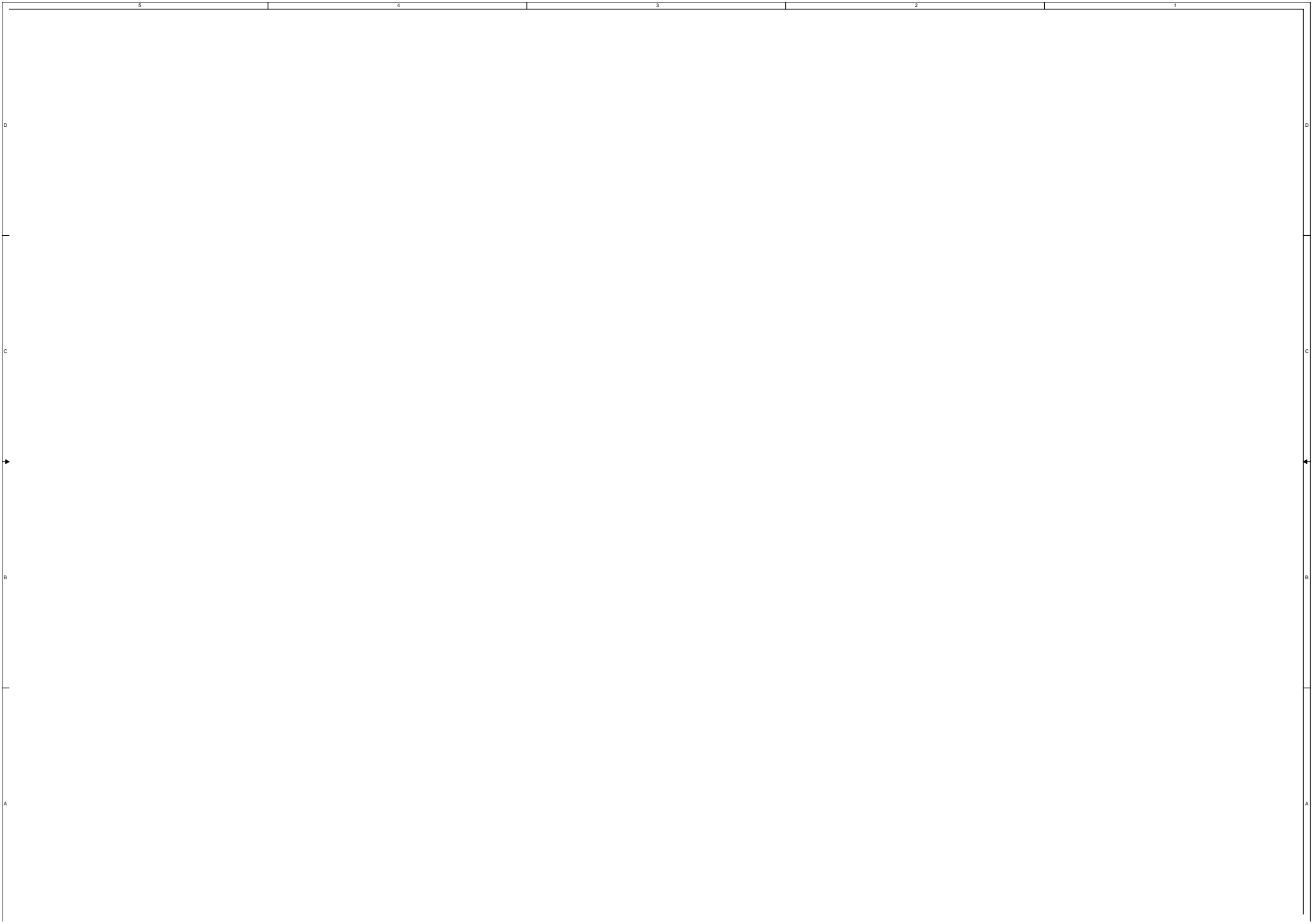


A		B		C		D		E	
1									1
2									2
3									3
4									4
5									5
PROJECT: Lanai		REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 25 OF 68	DESCRIPTION:		SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName>	DESIGN ENGINEER :	
A		B		C		D		E	

PROJECT: <b>Lanai</b>	REVISION	DATE: <b>Monday, March 19, 2007</b>	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	<b>1.2</b>	SHEET <b>26</b> OF <b>68</b>		RELEASE DATE :	

5		4		3		2		1	
D									D
C									C
B									B
A									A
PROJECT: Lanai									
REVISION		DATE: Monday, March 19, 2007		DESCRIPTION:		SCHEMATIC FILE NAME :		DESIGN ENGINEER :	
1.2		SHEET 27 OF 68				RELEASE DATE :		Sean Kuo	
5		4		3		2		1	







### SATA Connector

The diagram illustrates the pin configuration for a SATA connector. It shows the connection of power pins (1, 14, 15, 16) to +5V\_HDD and +3.3V\_RUN, and data pins (2-7, 11-13, 17-19) to SATA\_RXN0\_C, SATA\_RXP0\_C, and SATA\_RXN0+, SATA\_RXP0+.

**Component Values:**

- C58: 0.1uF/10V/Y5V
- C46: 1000PF/50V
- MLCC: +/-80-20%
- MLCC: +/-10%

**Component Placement Note:**

Place caps close to connector.

**Pin Configuration:**

Pin	Signal	Value
1	+5V_HDD	
2	SATA_RXN0_C	
3	SATA_RXP0_C	
4	SATA_RXN0_C	
5	SATA_RXP0_C	
6	SATA_RXN0_C	
7	SATA_RXP0_C	
8	+3.3V_RUN	
9		
10		
11		
12		
13		
14	+5V_HDD	
15		
16		
17		
18		
19		
20		
21		
22		

**Component Placement:**

SATA\_CON\_22P  
FOXCONN/LD2822H-SA3L6

**Component Values:**

- C319: 3900PF/50V/X7R
- C318: 3900PF/50V/X7R

**Component Placement Note:**

Place caps close to connector.

**Pin Configuration:**

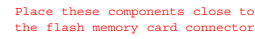
Pin	Signal	Value
1	SATA_RXN0_C	
2	SATA_RXP0_C	
3	SATA_RXN0+	
4	SATA_RXP0+	

[illegible]

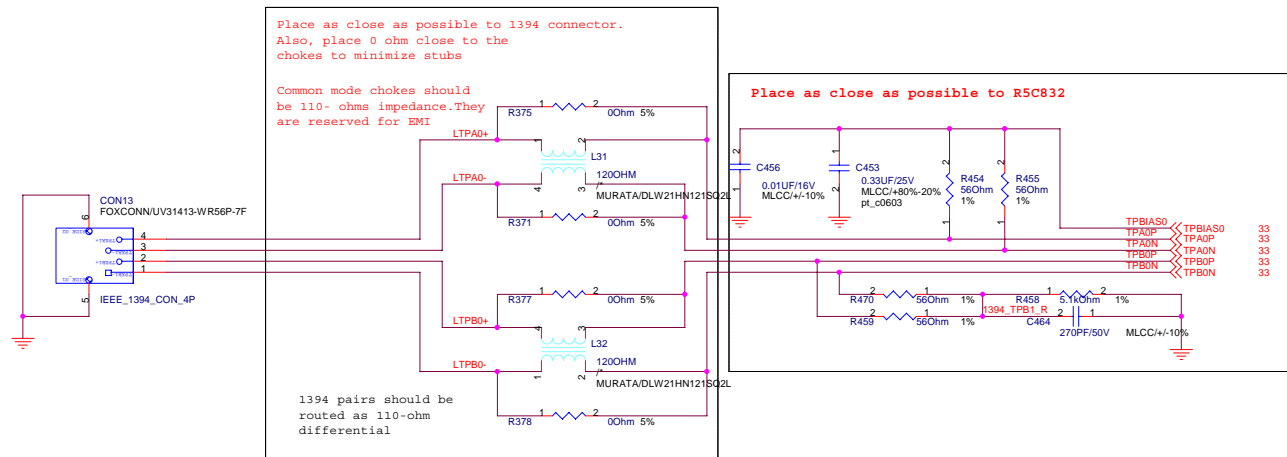
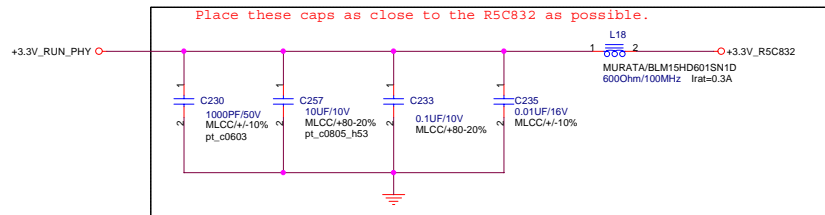




Normal Frequency : 24.576 MHz  
Frequency Tolerance : +/- 50ppm @ 25C  
Driver Level : .1 mW  
Load capacitance: 10pF  
Equ. Resistance : 50 Ohm Max  
Shunt Capacitance : 7.0pF Max



PROJECT: <b>Lanai</b>	REVISION	DATE: <b>Monday, March 19, 2007</b>	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	<b>1.2</b>	SHEET <b>33</b> OF <b>68</b>	<b>R5C833 - FLASH MEMORY PART</b>	RELEASE DATE :		



PROJECT: Lanai

REVISION  
1.2

DATE: Monday, March 19, 2007  
SHEET 34 OF 68

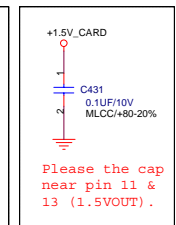
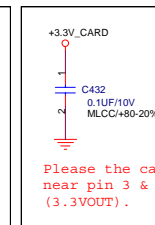
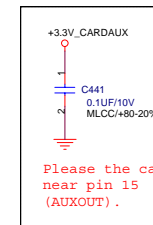
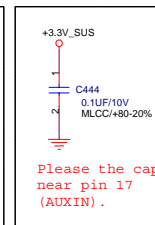
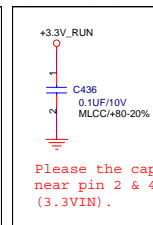
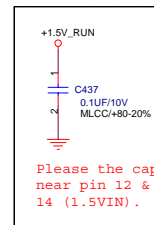
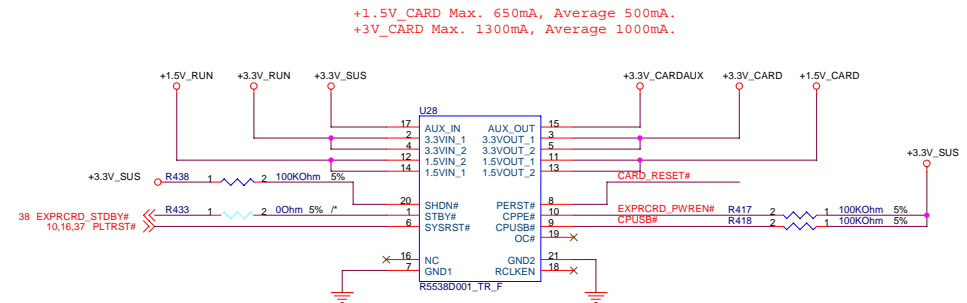
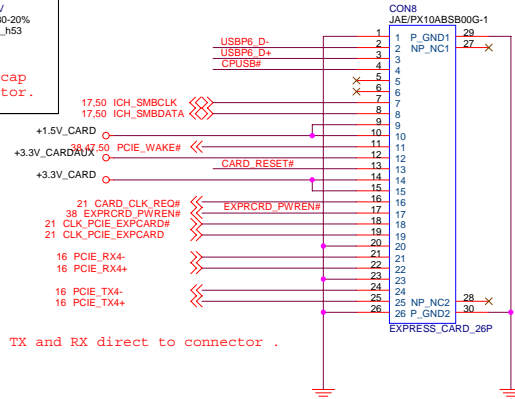
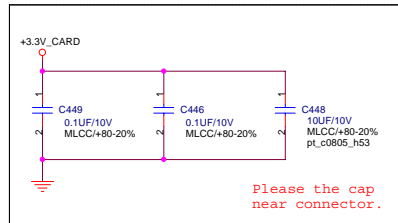
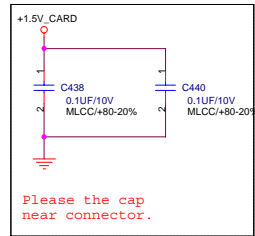
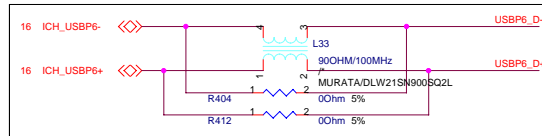
DESCRIPTION:  
R5C833 - IEEE1394 PART

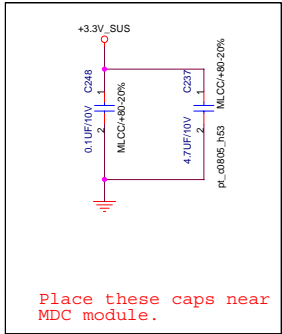
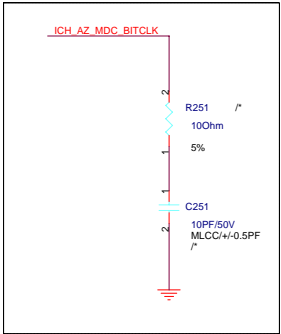
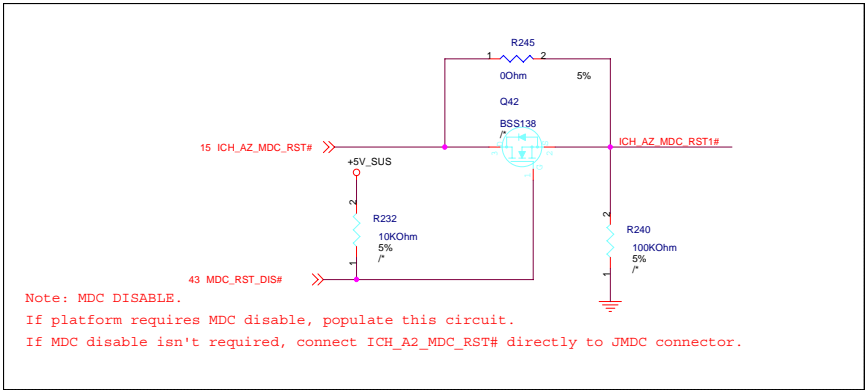
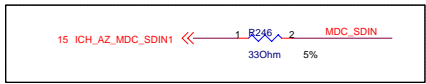
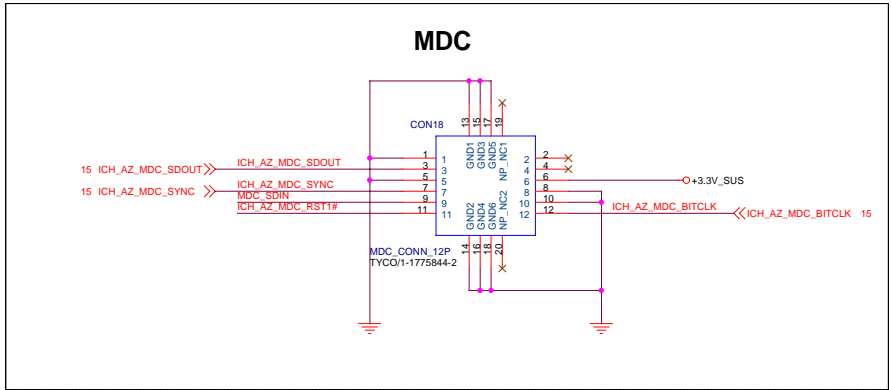
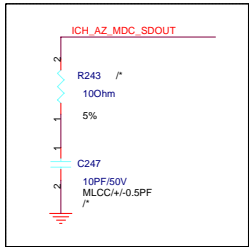
SCHEMATIC FILE NAME :  
RELEASE DATE :

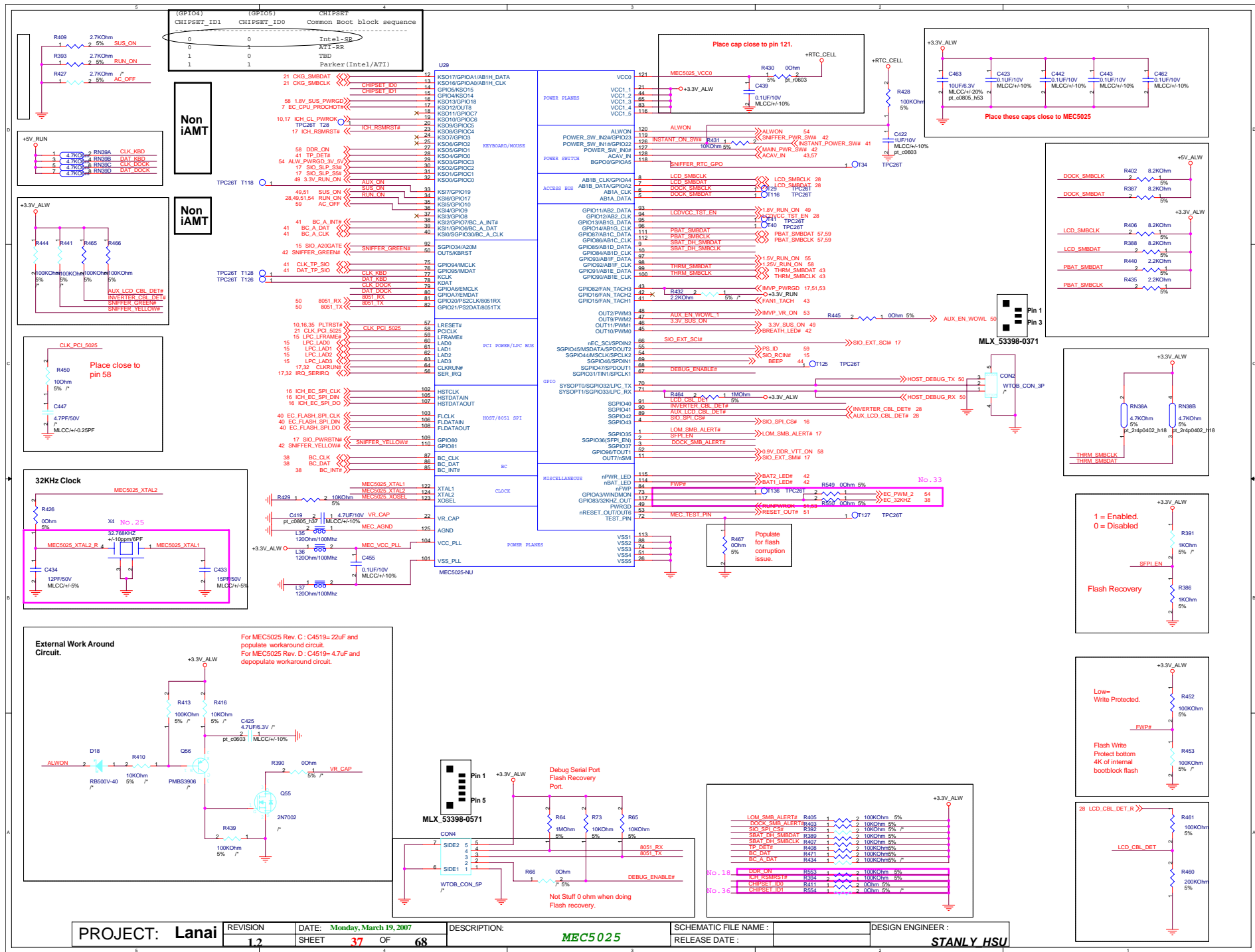
<OrgName>

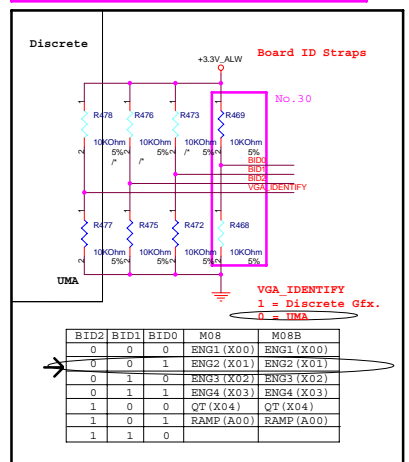
DESIGN ENGINEER :

## Express Card

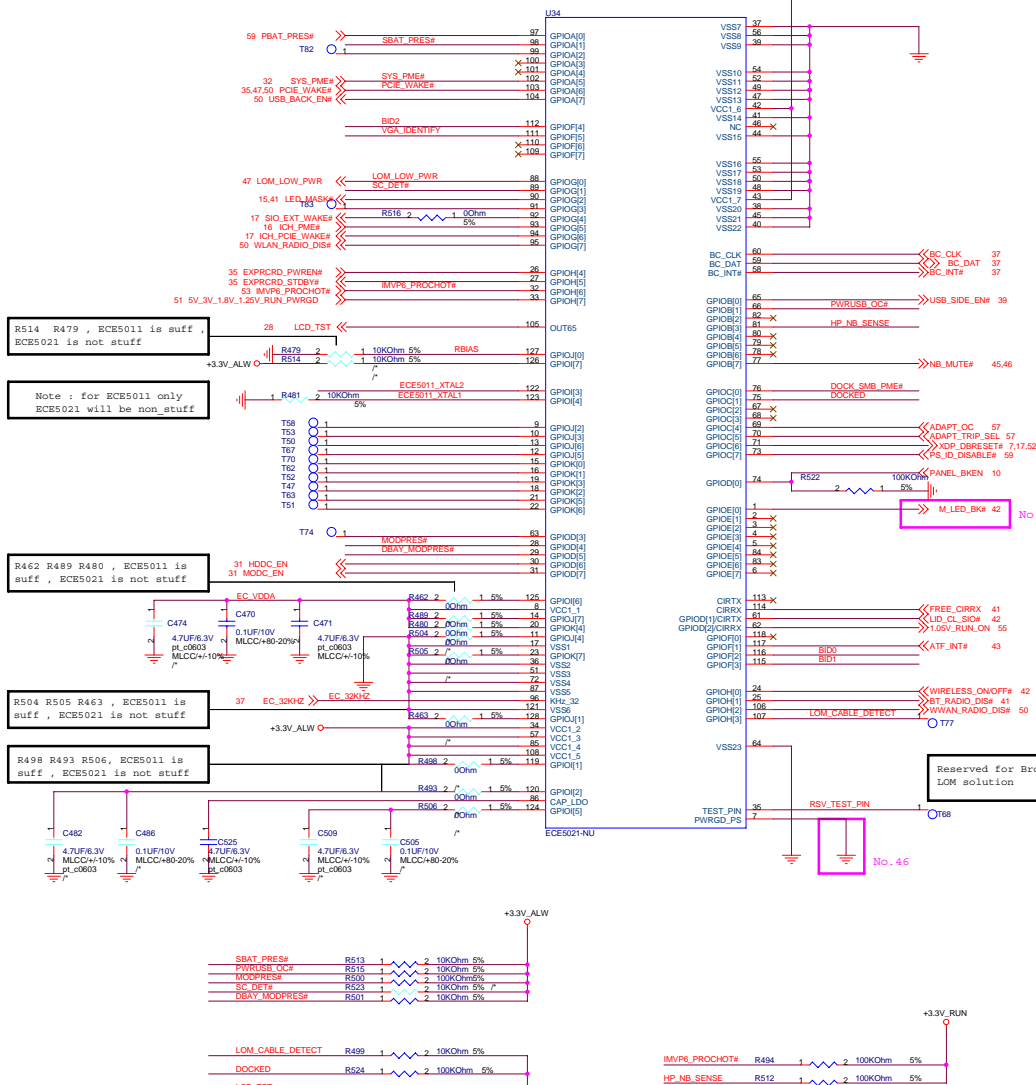
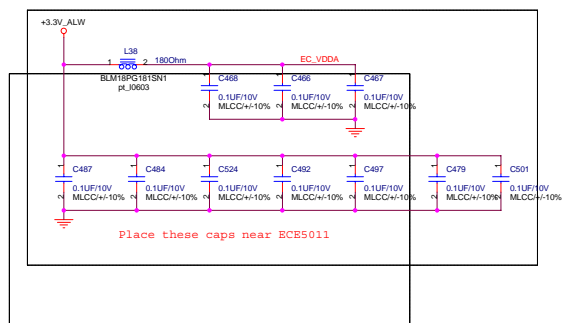
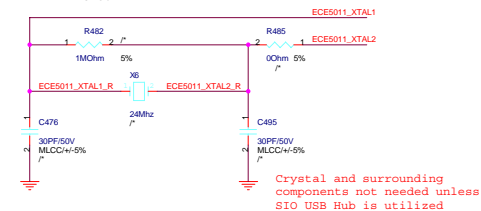


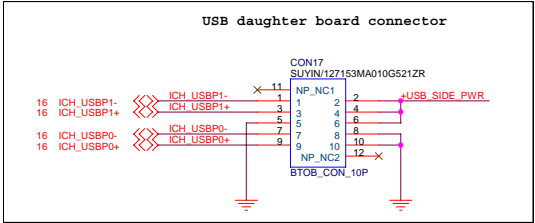
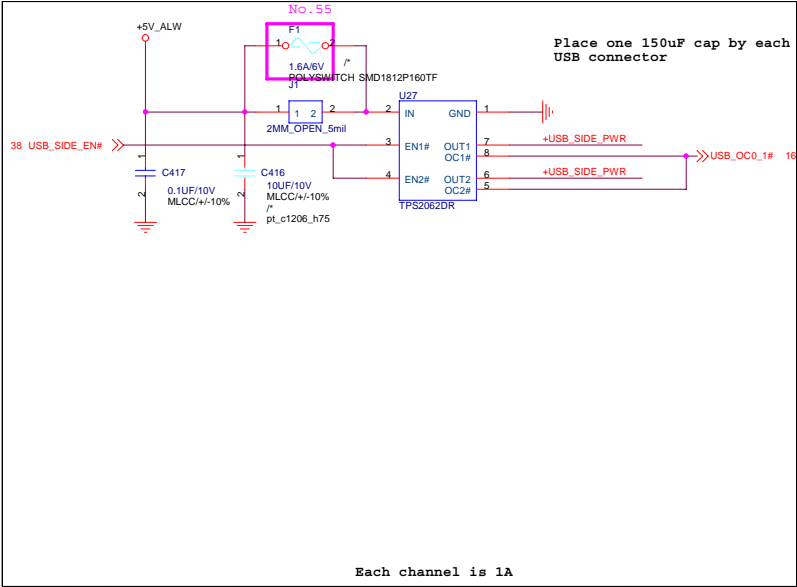






24MHz Clock





PROJECT: Lanai

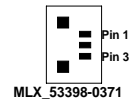
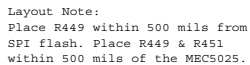
REVISION  
1.2

DATE: Monday, March 19, 2007  
SHEET 39 OF 68

DESCRIPTION:  
USB PORT x 2

SCHEMATIC FILE NAME : <OrgName>  
RELEASE DATE :

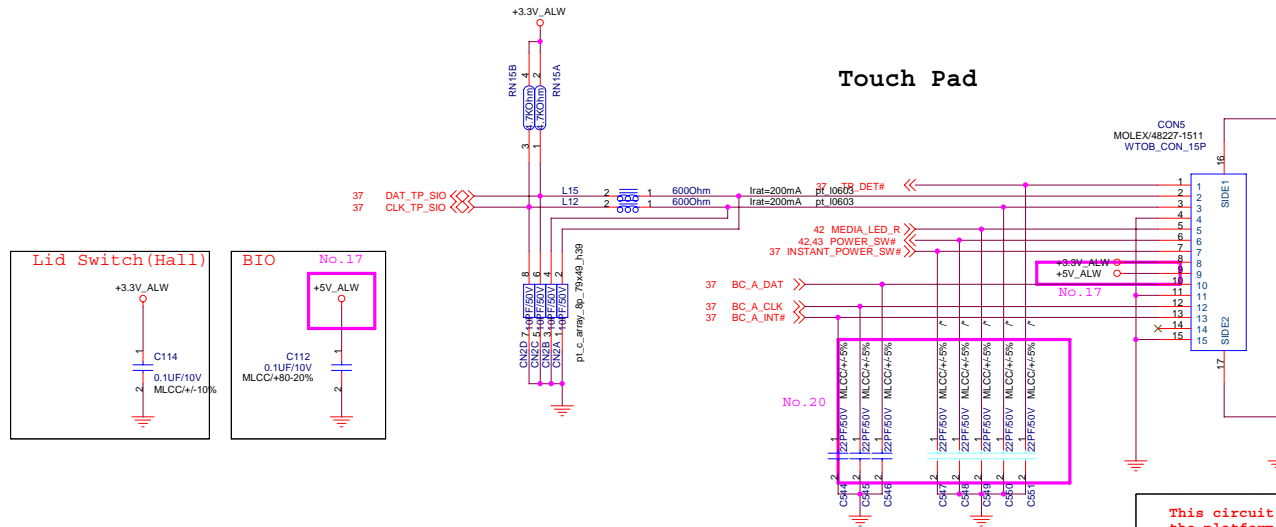
DESIGN ENGINEER :  
Terry Lin



PROJECT: <b>Lanai</b>	REVISION	DATE: <b>Monday, March 19, 2007</b>	DESCRIPTION: <b>FLASH &amp; RTC</b>	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : <b>C.L. Ho</b>
	<b>1.2</b>	SHEET <b>40</b> OF <b>68</b>		RELEASE DATE :		

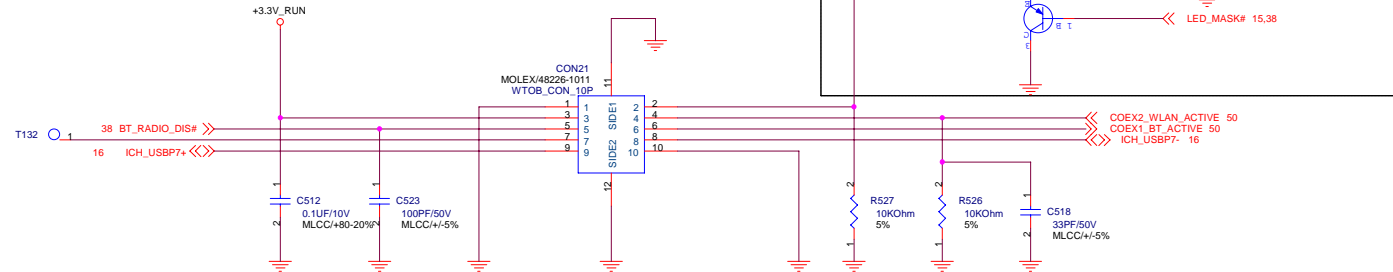


## Touch Pad



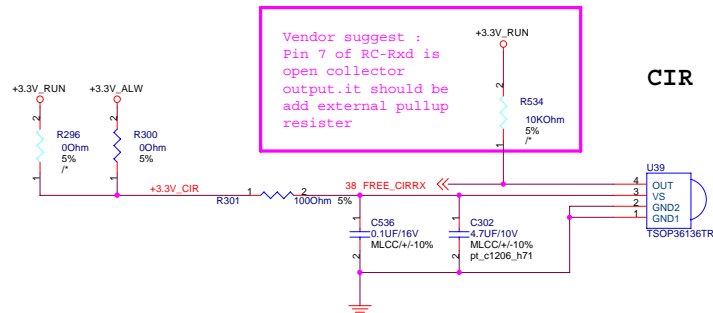
Please refer to item 191 of issue\_list\_0517\_TDC ,  
"Lanai plan to use 3V TP controller. No need  
TP\_VCC ". So we delete this circuit which  
supply TP\_VCC power.

## Bluetooth



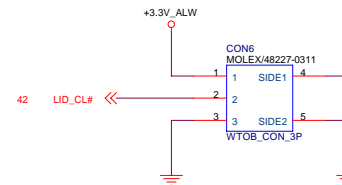
This circuit is only needed if  
the platform has the SNIFFER.

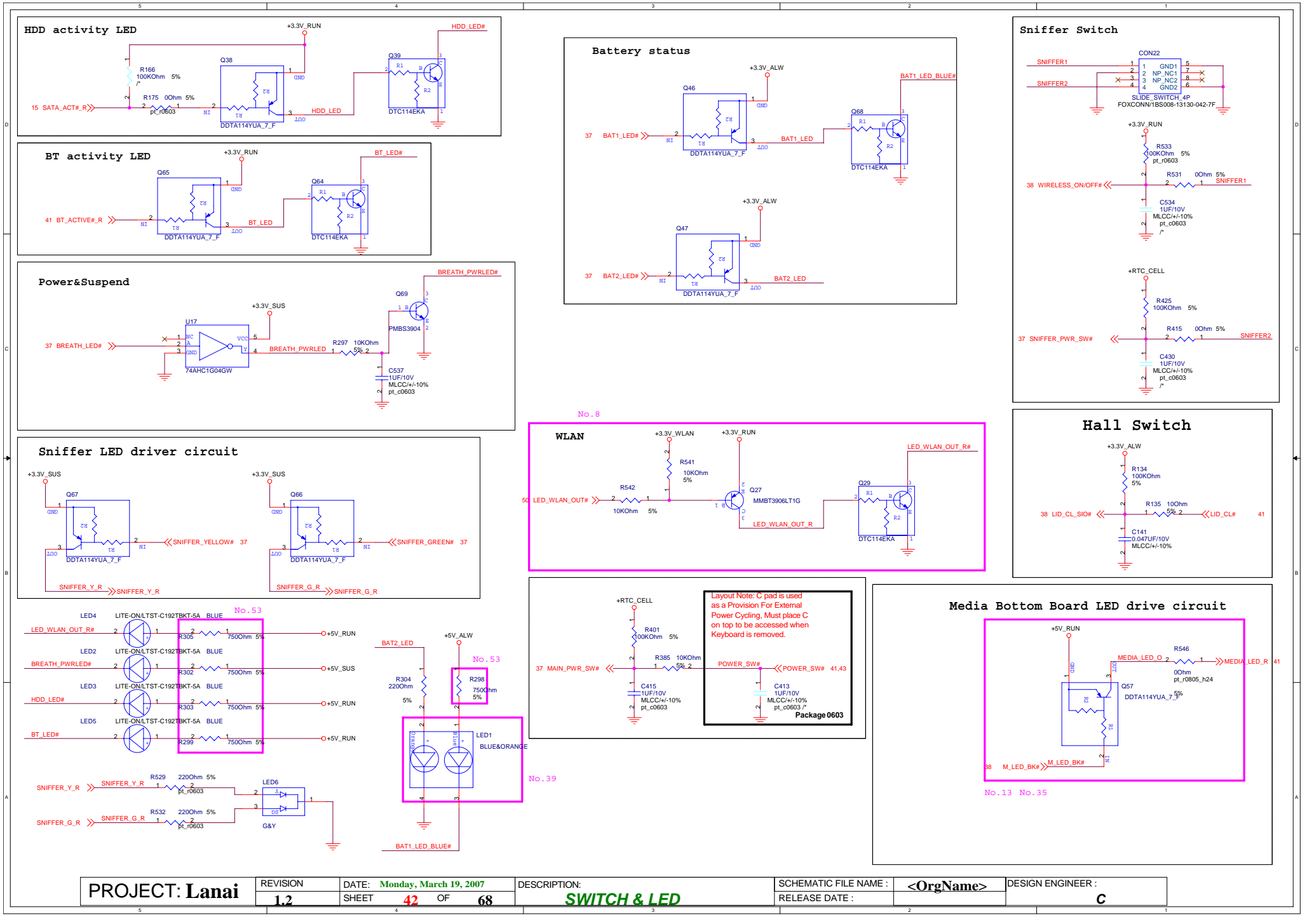
## CIR

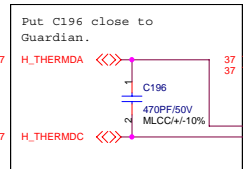
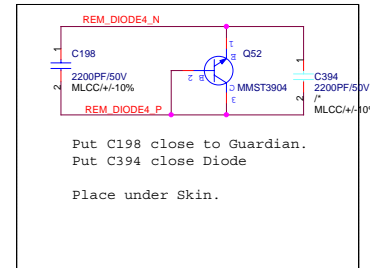
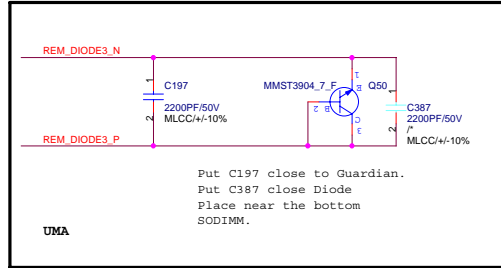
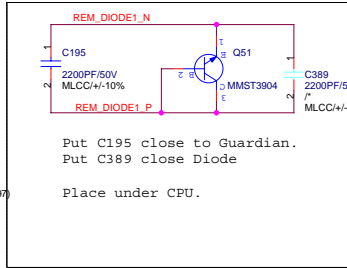
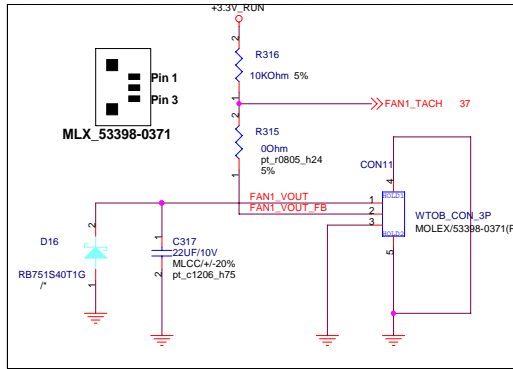


Vendor suggest :  
Pin 7 of RC-Rxd is  
open collector  
output.it should be  
add external pullup  
resister

## HALL SENSOR

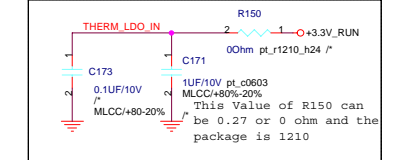
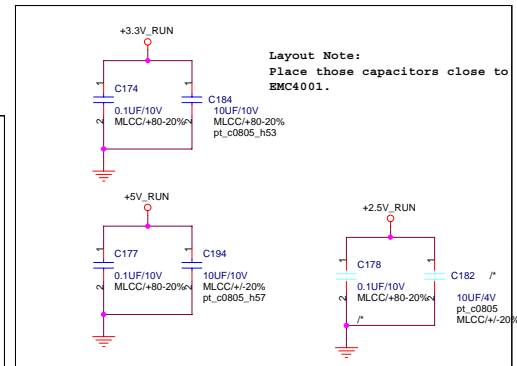
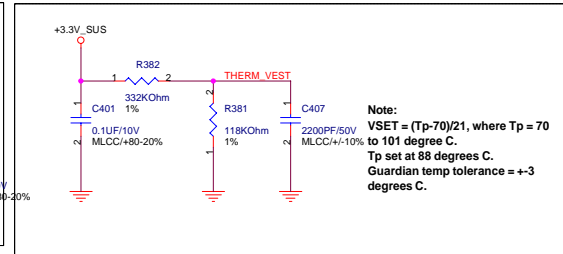
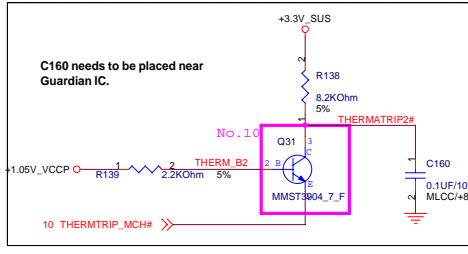
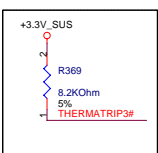
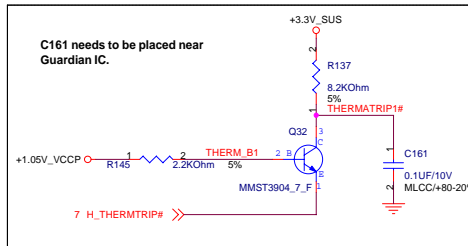
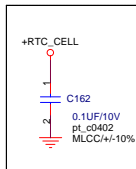
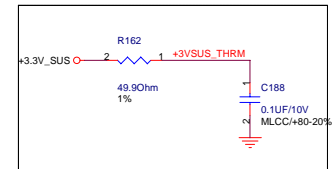
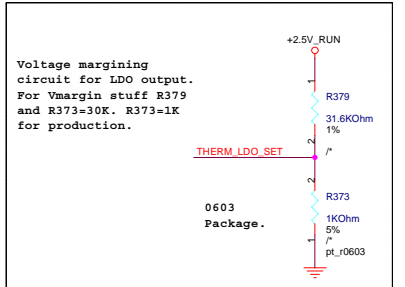
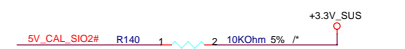
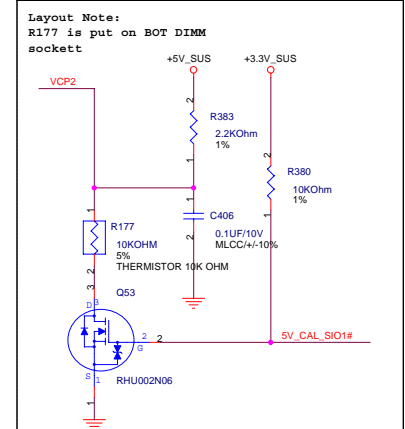
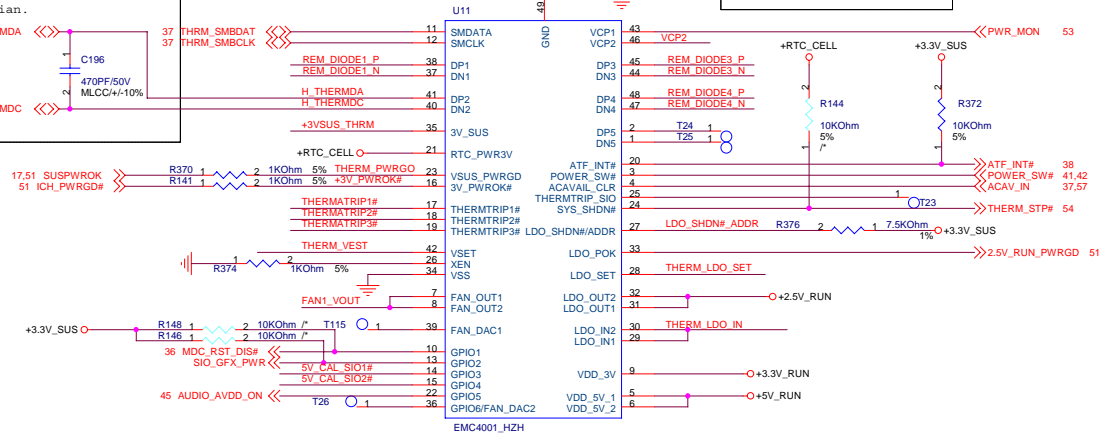






## Guardian

Note:  
150K input impedance on VCP1 (Pin 43)



PROJECT: Lanai

REVISION 1.2

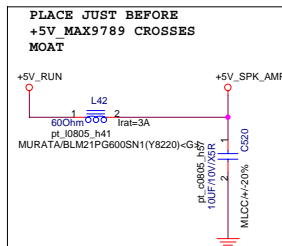
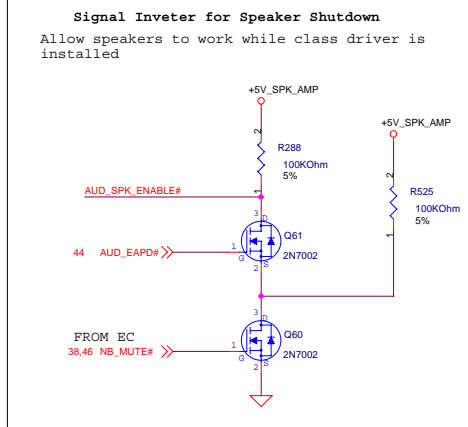
DATE: Monday, March 19, 2007  
SHEET 43 OF 68

DESCRIPTION: EMC4001

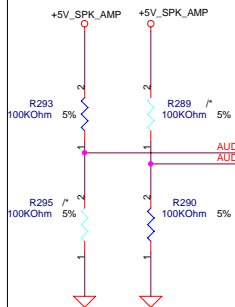
SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER : N

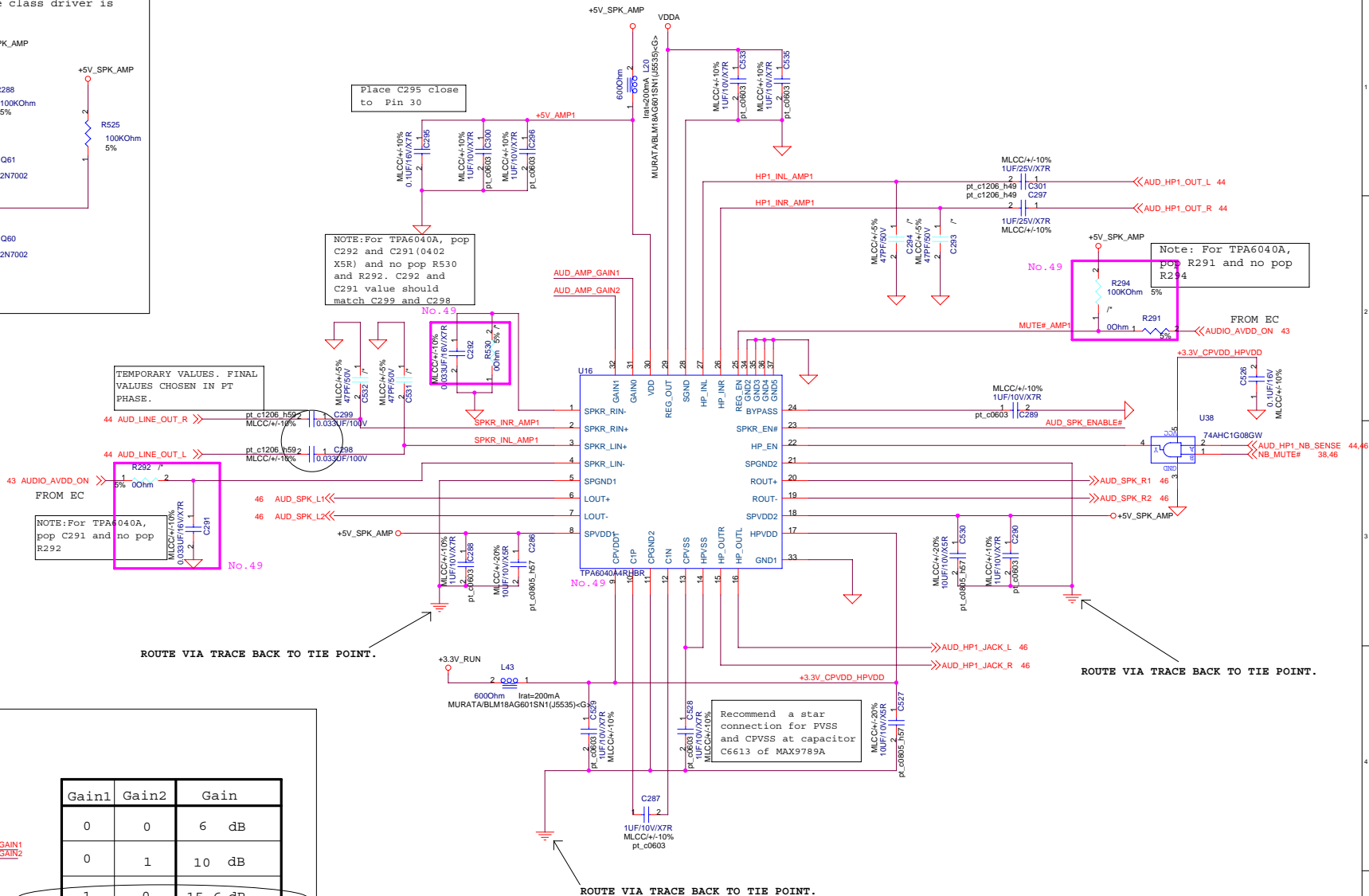




#### GAIN SETTING RESISTORS



Gain1	Gain2	Gain
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



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DATE: Monday, March 19, 2007  
SHEET 45 OF 68

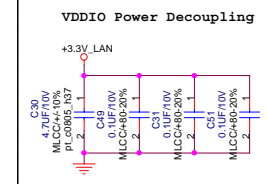
DESCRIPTION:

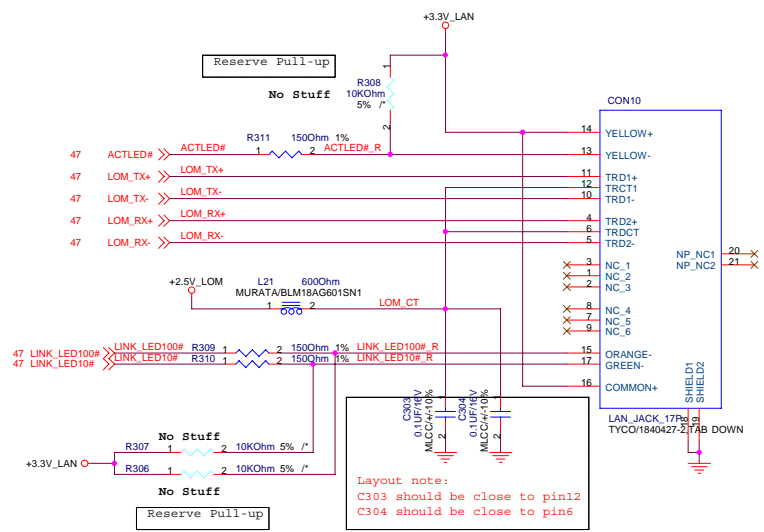
AMP MAX9789

SCHEMATIC FILE NAME : <OrgName>  
RELEASE DATE :

DESIGN ENGINEER :  
Yihao Yeh

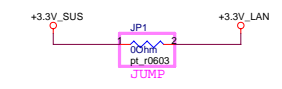






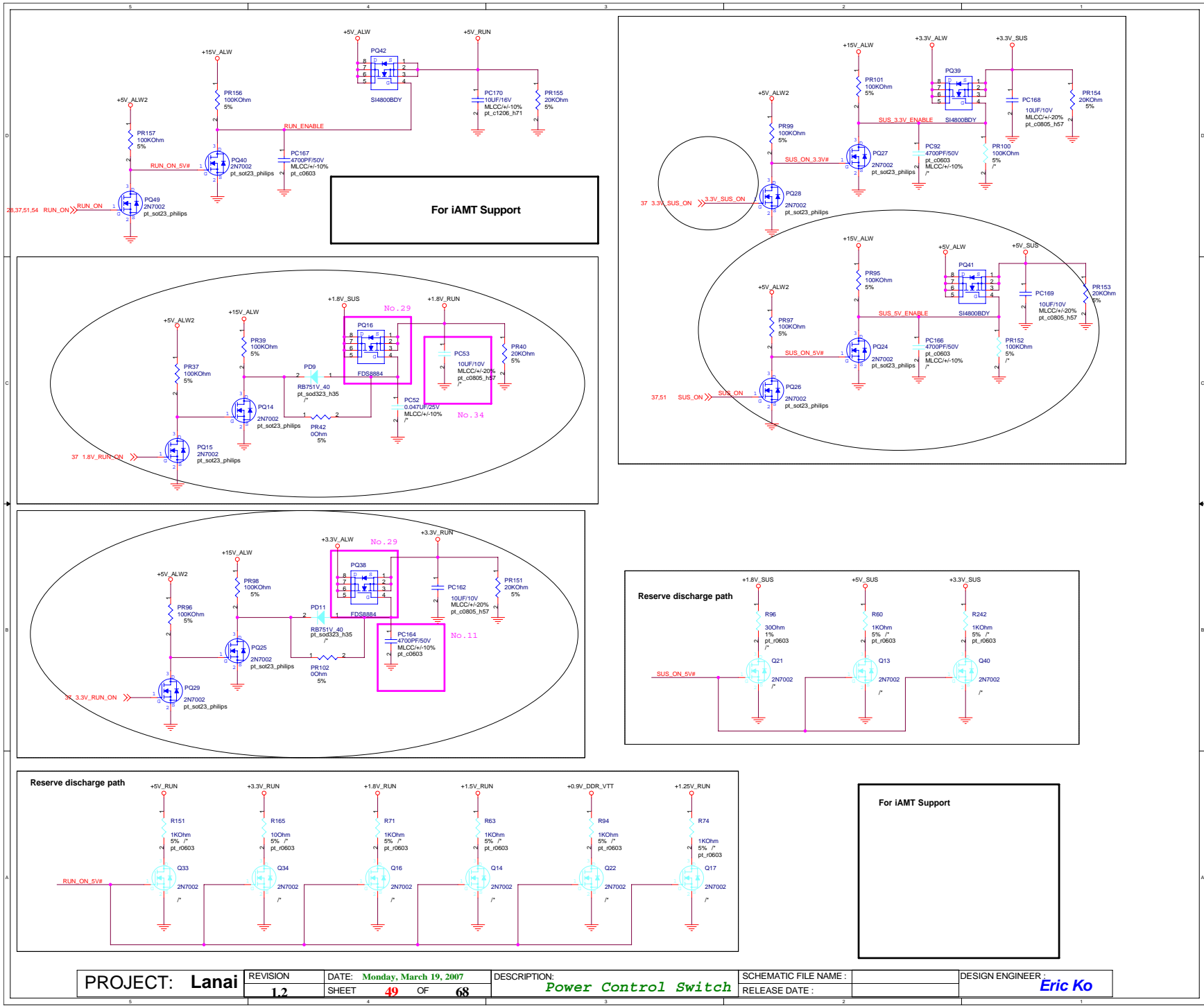
### +3.3V LAN Source Guideline:

1. Use +3.3V\_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V\_SRC if Wake-on-LAN is required out of S4, S5



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: Magnetics and RJ-45	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
	1.2	SHEET 48 OF 68			
				RELEASE DATE :	Ivan Chou





PROJECT: Lanai

REVISION  
1.2

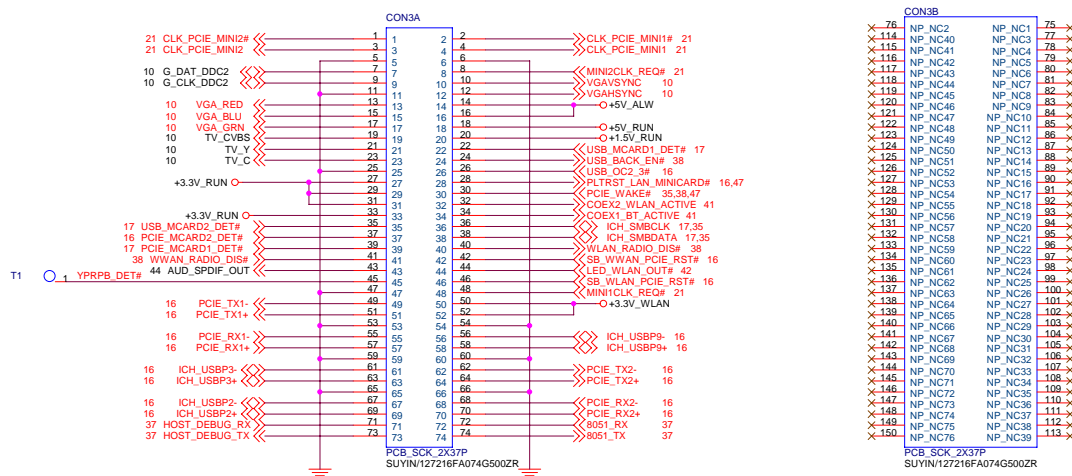
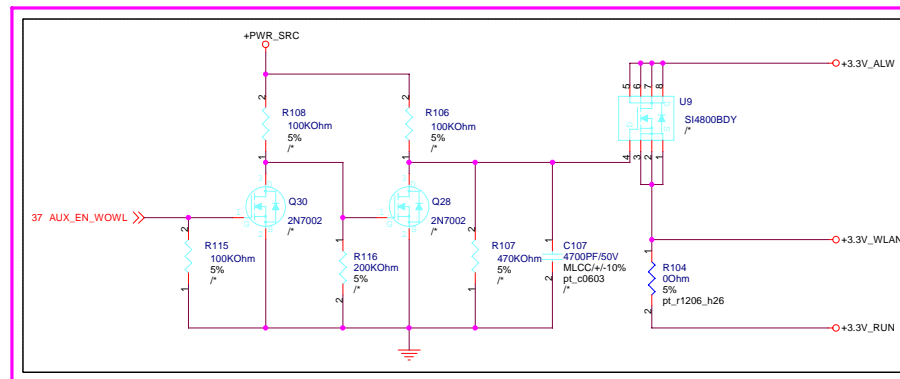
DATE: Monday, March 19, 2007  
SHEET 49 OF 68

DESCRIPTION:  
Power Control Switch

SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER :  
Eric Ko

No. 21



PROJECT: Lanai

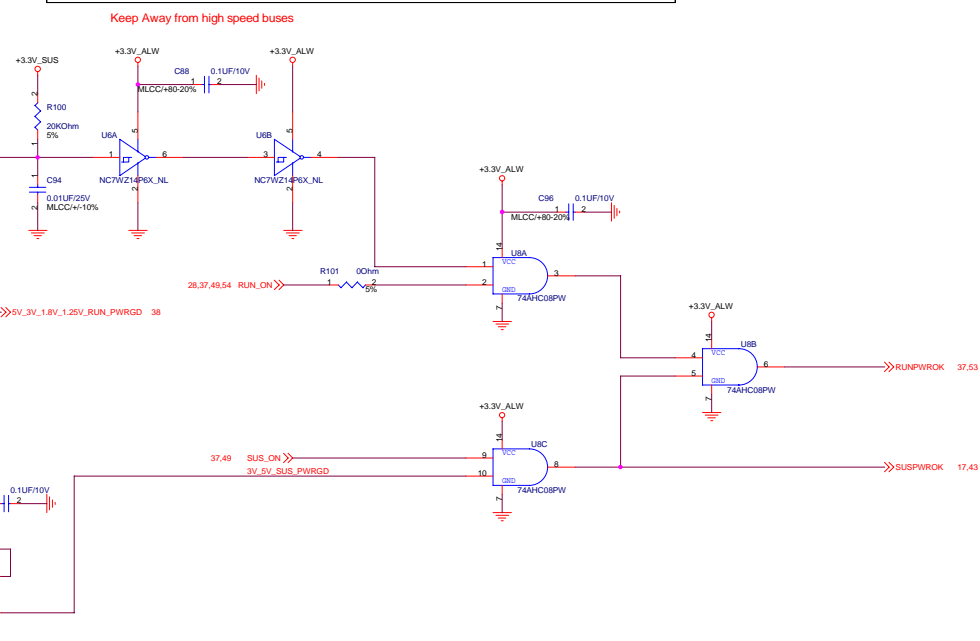
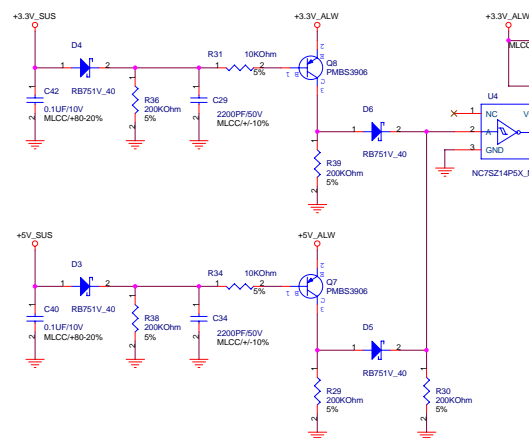
REVISION  
1.2

DATE: Monday, March 19, 2007  
SHEET 50 OF 68

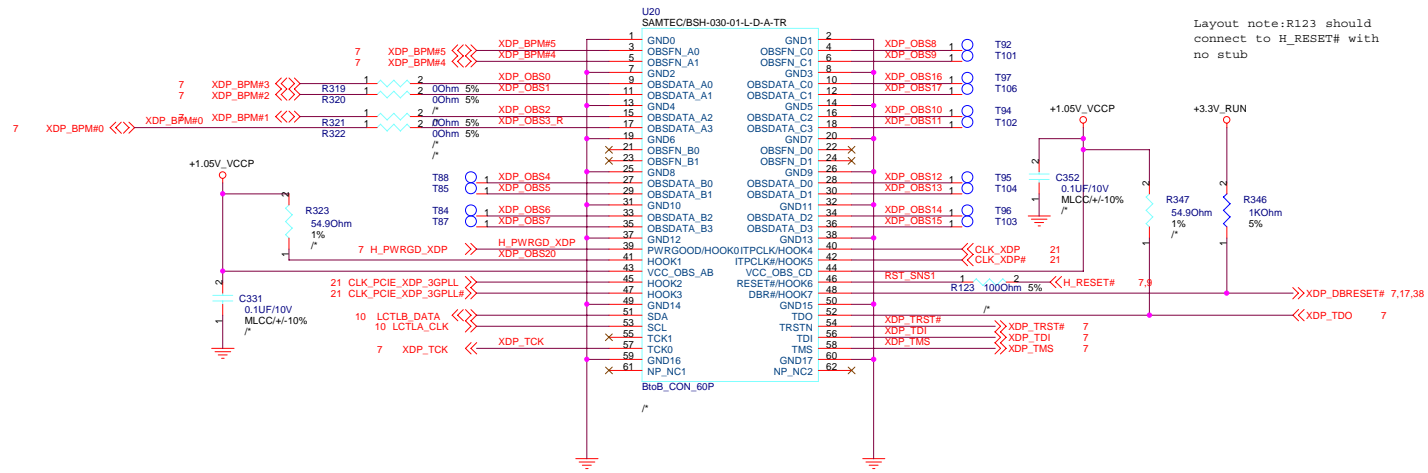
DESCRIPTION: BtoB CON

SCHEMATIC FILE NAME : <OrgName>  
RELEASE DATE :

DESIGN ENGINEER :  
STANLY HSU



# XDP



CAD NOTE:  
Place the XDP connector on the primary side of the CRB and place all components near the connector.

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: XDP	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : Terry Lin
	1.2	SHEET 52 OF 68		RELEASE DATE :		

Design Current: 35.2A  
Maximum current: 44A  
OCP point min. 50A

PROJECT: Lanai

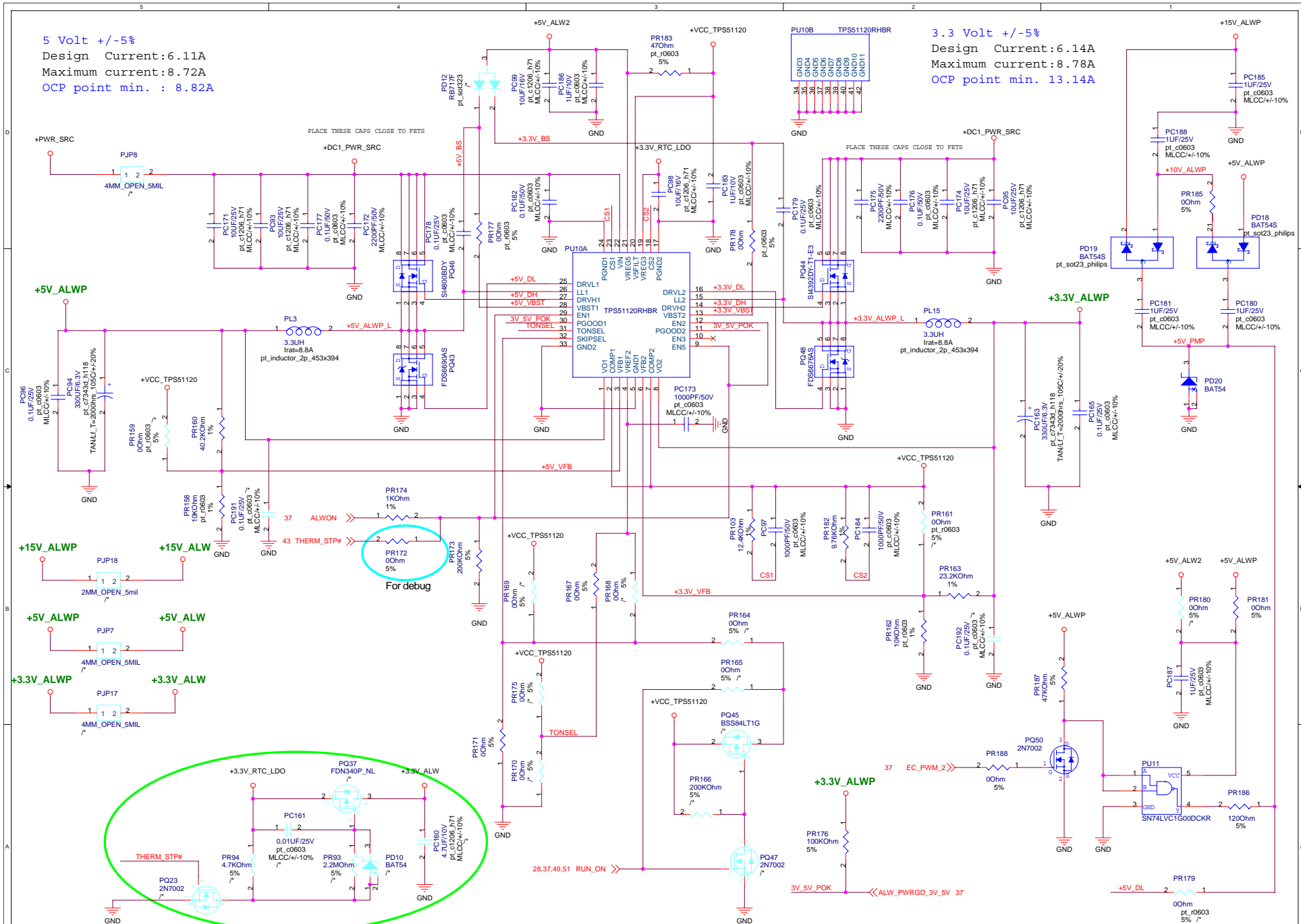
REVISION	DATE	DESCRIPTION	SCHEMATIC FILE NAME	DESIGN ENGINEER
1.2	Monday, March 19, 2007	POWER_VCORE	<OrgName>	JEFF

SHEET 53 OF 68

PROJECT: <b>Lanai</b>	REVISION	DATE: <b>Monday, March 19, 2007</b>	DESCRIPTION: <b>POWER_VCORE</b>	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : <b>JEFF</b>
	<b>12</b>	SHEET <b>53</b> OF <b>68</b>		RELEASE DATE :		

5 Volt +/-5%  
Design Current:6.11A  
Maximum current:8.72A  
OCP point min. : 8.82A

3.3 Volt +/-5%  
Design Current:6.14A  
Maximum current:8.78A  
OCP point min. 13.14A



PROJECT: **Lanai**

REVISION
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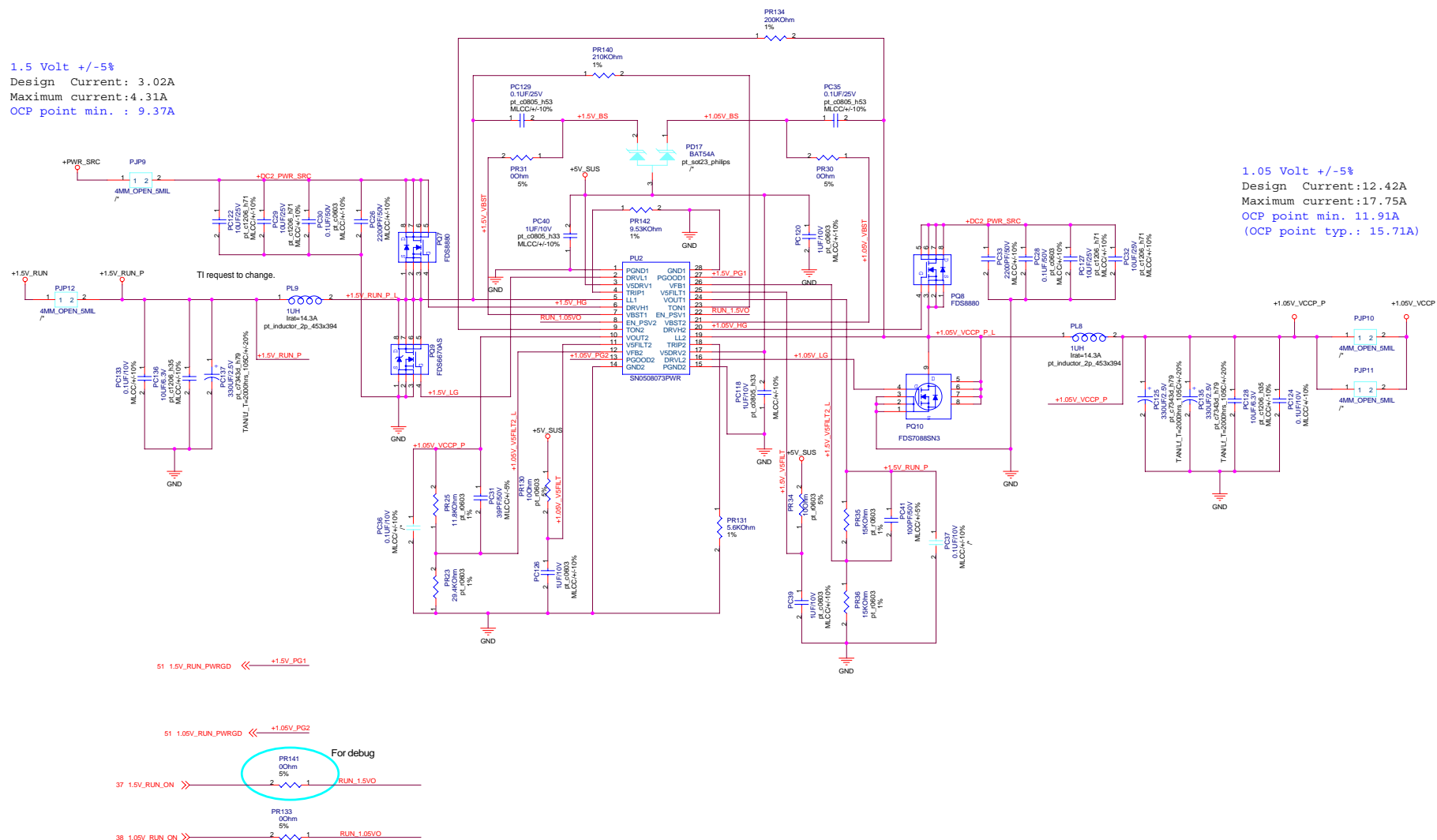
DATE:	Monday, March 19, 2007		
SHEET	54	OF	68

DESCRIPTION:	POWER_SYSTEM5V_ALW&3.3V_ALW
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SCHEMATIC FILE NAME :	<OrgName>
RELEASE DATE :	

DESIGN ENGINEER :	<b>JEFF</b>
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1.5 Volt +/-5%  
Design Current: 3.02A  
Maximum current:4.31A  
OCP point min. : 9.37A



1.05 Volt +/-5%  
Design Current:12.42A  
Maximum current:17.75A  
OCP point min. 11.91A  
(OCP point typ.: 15.71A)

PROJECT: <b>Lanai</b>	REVISION	DATE: <b>Monday, March 19, 2007</b>	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	<b>12</b>	SHEET <b>55</b> OF <b>68</b>	<b>POWER I/O 1.5VS &amp; 1.05VS</b>	RELEASE DATE :		<b>JEFF</b>





TOTAL POWER=65W  
-->3.34A

TABLE3 PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSOP
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT
"NC" means no-connect		

Charge Current:4.68A  
Discharge current:6.6A

TABLE2 MAXIM & INTERSIL BOM DIFFERENCES		
REF DES	MAXIM	INTERSIL
PR125	8.45K, 0402, 1%	16.0K, 0402, 1%
PC115	0.01uF	No Stuff
PC17	0.1uF, 0402, 10V	No Stuff
PC24	1.0uF, 0603, 10V	No Stuff
PR106	365K, 0402, 1%	215K, 0402, 1%
PR8	0, 0402, 5%	10, 0402, 5%
PR21	0, 0402, 5%	10, 0402, 5%
PC4	No Stuff	0.22uF
PC19	No Stuff	0.22uF
PC22	0.01uF	No Stuff
PC18	0.1uF, 0402, 10V	No Stuff
PC8	220pF, 0402, 50V	No Stuff
PD16	RB751V-40	No Stuff
PC13	3.3nF	No Stuff
PR19	1, 0603, 1%	0, 0603, 5%
PR9	100, 0402, 5%	0, 0402, 5%
PR22	4.7K, 0402, 5%	4.7K, 0402, 5%
PC23	0.01uF	0.01uF
PC21	0.01uF	0.01uF
PD3	1SS355	No stuff
PR12	1K, 0603, 5%	No stuff

TABLE1				
ADAPTOR (W)	TRIP CURRENT (A)	PR121	PR123	PR126
65	3.17	57.6K	13.0K	105
90	4.43	51.1K	17.8K	348
130	6.43	32.4K	20.5K	100
150	7.43	30.9K	24.9K	432
200	9.75	19.1K	28K	301
230	11.28	32.4K	6.49K	115

Note 1: PR122 is populated if ADAPT TRIP SET is used to program for the next lower adaptor  
ADAPT TRIP SET is floating for the higher adaptor, grounded for the lower adaptor  
Note 2: 24.9K at PR122 allows the 65W adaptor setting to switch down to 45W. (now is N/A)  
Note 3: PR109 must be 5m ohm instead of 10m ohm for the 230W adaptor

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DATE: Monday, March 19, 2007  
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DESCRIPTION: POWER CHARGER

SCHEMATIC FILE NAME:  
RELEASE DATE:

<OrgName>

DESIGN ENGINEER:  
JEFF

1.25Volt +/-5%  
Design Current:0.93A  
Maximum current:1.33A  
OCP point min. : 6.54A

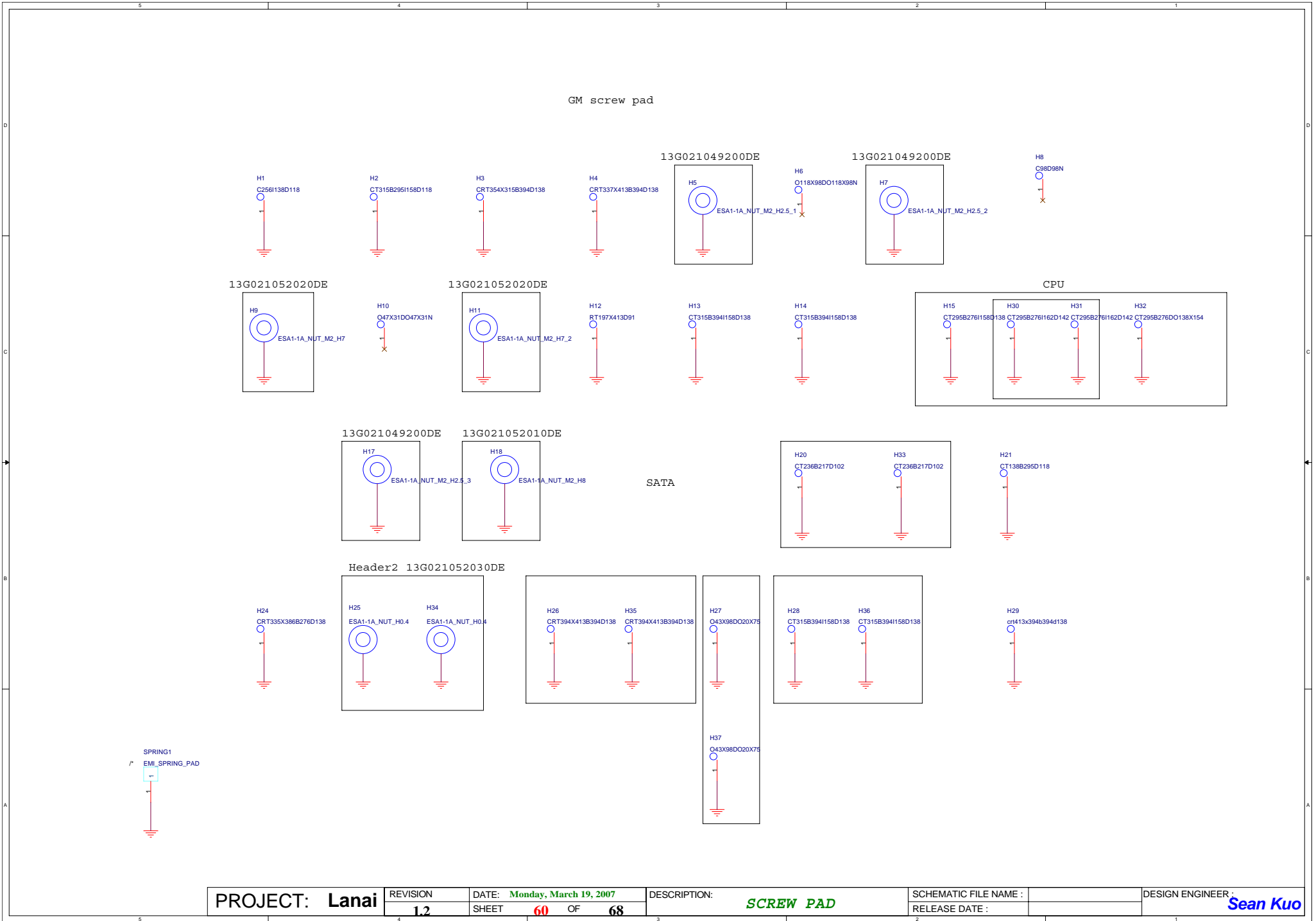
1.8Volt +/-5%  
Design Current: 6.59A  
Maximum current: 9.42A  
OCP point min. : 16.93A

0.9Volt +/-5%  
Design Current:1.05A  
Maximum current:1.5A

No. 32

[illegible]





PROJECT: Lanai

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DATE: Monday, March 19, 2007  
SHEET 60 OF 68

DESCRIPTION: SCREW PAD

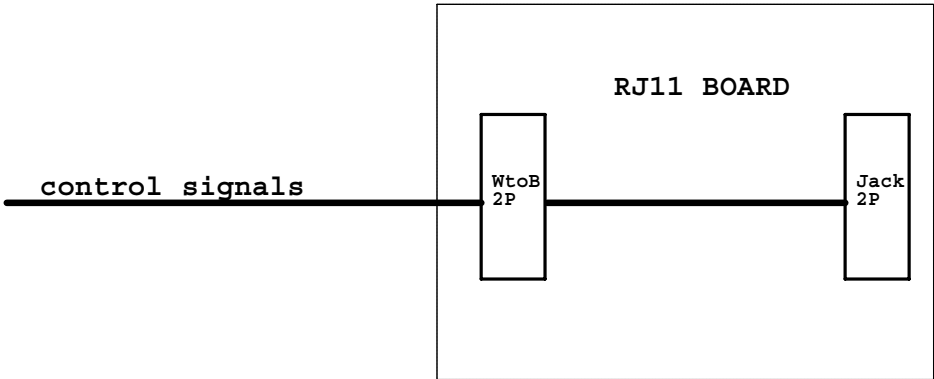
SCHEMATIC FILE NAME :  
RELEASE DATE :

DESIGN ENGINEER : Sean Kuo

ASUS CONFIDENTIAL

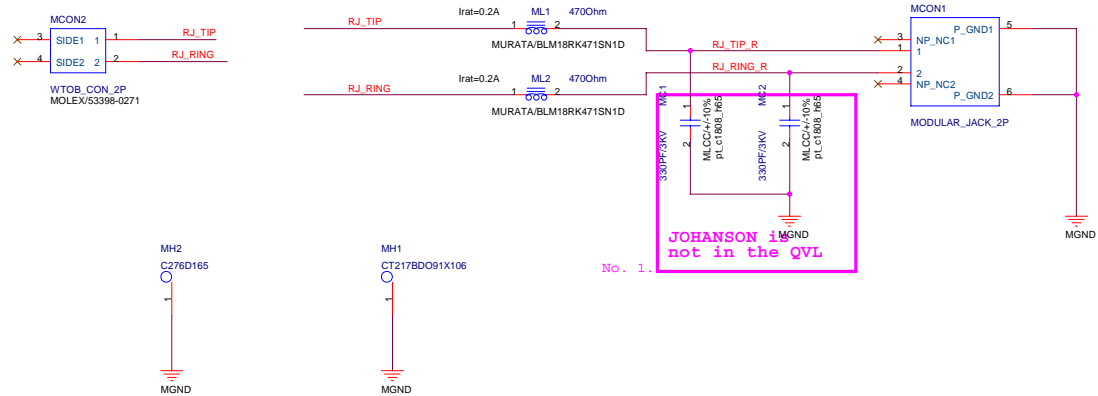
MODEL NAME : *Elsa*

*Lanai:Modem Board*



**REV : 1.1(DELL: X01)**

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 64 OF 68	BLOCK DIAGRAM	RELEASE DATE :	Stanly Hsu



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: RJ-11 CONN	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
	1.2	SHEET 65 OF 68			
				RELEASE DATE :	Stanly Hsu

ASUS CONFIDENTIAL

MODEL NAME : *Elsa*  
PCB NO : *???*  
ASUS P/N : *???*

Lanai PP2 USB Board

REV : 1.1(DELL: X01)

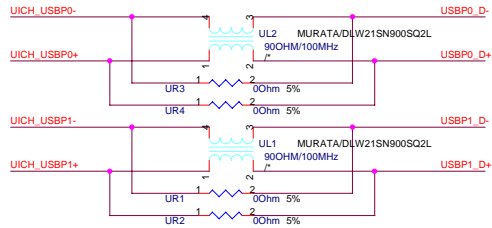
MB PCB

Part Number	Description
DA800004H0L	PCB 00B LA-3071P REV0 M/B

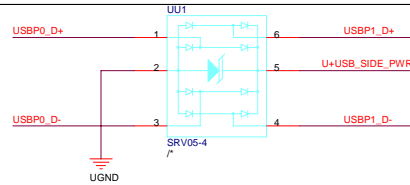
*BOM NO. ???*  
*PCB P/N: ???*

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: Cover Page	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Terry Lin
	1.2	SHEET 67 OF 68		RELEASE DATE :	

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

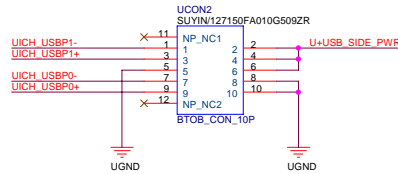


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C ( 1pf vs 3pf ) .

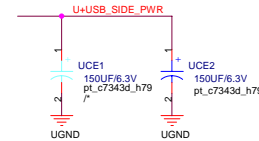
#### USB daughter board connector



#### Screw hole

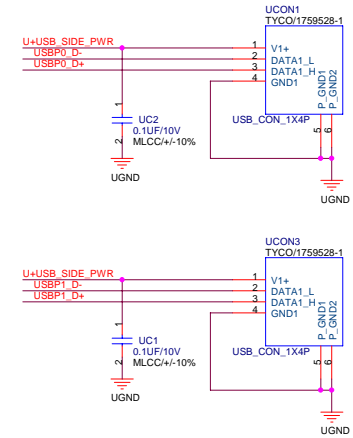


Place one 150uF cap by each USB connector



Each channel is 1A

Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines.  
Add PADS ONLY until proven diodes are really needed.



PROJECT: Lanai

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DATE: Monday, March 19, 2007  
SHEET 68 OF 68

DESCRIPTION:  
USB PORT ( SINGLE \* 2 )

SCHEMATIC FILE NAME :  
RELEASE DATE :

<OrgName>

DESIGN ENGINEER :  
Terry Lin